Design and Implementation of Finite State Machine Decoders for Phase Disposition Pulse Width Modulation of Modular Multilevel Converters

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Abstract — It is well known that level shifted phase disposition pulse width modulation (PD-PWM) achieves the best possible three-phase line-to-line output voltage spectrum for multilevel converters. However, the strategy does require post modulation signal decoding to optimally select between redundant switched states and to achieve an even distribution of commutation events across all switching devices. For modular multilevel converters (MMCs), PD-PWM involves firstly scheduling the individual module switching events of both arms as an integrated process to achieve optimal harmonic performance and, then selecting between redundant states to balance the individual module capacitor voltages, and to also minimise the phase leg high frequency circulating currents. This paper discusses the design and implementation of finite state machine PD-PWM post modulator decoders for MMCs to achieve these objectives. The proposed approach has been verified in simulation and then with experimental confirmation using a two module per arm MMC.

I. INTRODUCTION

The modular multilevel converter (MMC) is an attractive topology for medium/high voltage applications with large power conversion ratings [1]-[11], because of its scalability to high operating voltages via the series connection of 2N modules (N per arm), its ability to operate from a single DC link without bulk bus storage capacitors, and its capability to synthesise switched waveforms with low harmonic content [3] [4]. However, since a MMC can synthesise individual output voltage levels using multiple redundant switched states, appropriate selection of these states is required to simultaneously meet the three essential requirements of maintaining balance of the individual module DC link voltages [4] [5], evenly distributing device switching losses over each fundamental cycle [4], and minimising the circulating currents that flow between the upper and lower MMC arms of each phase leg to reduce device conduction and commutation loss [4] [5]. These competing requirements make modulation of a MMC a complex task, particularly when using the harmonically superior three-phase level-shifted phase disposition modulation (PD-PWM) [12].

PD-PWM switching signals are synthesised by comparing a fundamental sinusoidal reference against N smaller magnitude triangular carriers arranged continuously across the linear modulation range. This scheme is well-known to achieve the best possible converter line-to-line output voltage spectrum because significant energy is put into the first carrier harmonic, which is co-phasal between the phase legs of a three-phase system [12]. However, since PD-PWM does not differentiate between redundant switched states [13], it requires post modulation state selection to equally distribute switching events across all module semiconductor devices, and to control the converter phase leg circulating currents [14]. With this approach, MMCs can generate switched output voltages with 2N+1 levels using nearly all possible redundant states, or N+1 voltage levels when only a reduced set of redundant states are used.

Synthesis of optimal PD (2N+1 or N+1) switched output voltage levels for a MMC requires integrated scheduling of the individual module switching events for both arms [14]. In addition, for the 2N+1 PD scheme the redundant switched states must be carefully sequenced by the post modulator decoder to avoid disrupting the phase leg high-frequency circulating currents, particularly during band transitioning processes [13]. In contrast, for PD synthesis of N+1 switched output voltage levels, any form of round-robin redundant state sequencing is satisfactory, since the subset of redundant states used by this scheme has no effect on the phase leg circulating current. Based on these concepts, this paper presents design principles for developing 2N+1 and N+1 PD-PWM finite state machine decoders for modular multilevel converters. The work has been verified by simulations and experimental investigations on a N = 2 MMC.

II. EFFECT OF PHASE LEG SWITCHING ON MMC CIRCULATING CURRENT

The circuit topology of an exemplar MMC phase leg with two modules per arm is shown in Fig. 1. The overall converter phase leg consists of upper and lower arms, each formed by the series connection of two identical modules, with each arm linked to the phase leg output through an inductor. The individual modules have a complementary switch pair and a floating capacitor, which under steady-state balanced conditions is charged to V_{dc}/2. For generality, the arm inductors are considered as coupled (i.e. built on a common magnetic core) with winding leakage and mutual inductances L_k and L_b, and a small series resistance R_b per winding.

Table I shows the 16 possible phase leg switched states, denoted as C_{hex} for i = \{0, 1, 2, ..., 9, A, B, ..., F\}, that are defined by the binary combinations of the four individual converter module switching states defined by \(\sigma_{i,bin}\) for
From [6] [7] [14], the common-mode circulating current $i_{cm}$ is given by:

$$i_{cm} \approx \frac{1}{L_s + 2L_g} \int \left( \frac{V_o}{2} - v_{cm} \right) dt. \quad (1)$$

Depending on this common-mode voltage, the circulating current will vary between remaining constant when $v_{cm} = V_{dc}/2$, increasing at a given slope when $v_{cm} = V_{dc}/4$, decreasing at the same slope when $v_{cm} = 3V_{dc}/4$, and increasing or decreasing at twice that slope when $v_{cm} = 0V$ or $v_{cm} = V_{dc}$, respectively. This information is also illustrated graphically in the $i_{cm}$ column in Table I.

From Table I, there are 4 converter states available to produce the output voltage level $L_1$ (i.e. $v_o = V_{dc}/4$). Two of them generate a positive slope for the circulating current (states $C_4$ and $C_8$), and two create a negative slope for the circulating current (states $C_9$ and $C_{10}$). Similarly, the output voltage level $L_3$ (i.e. $v_o = -V_{dc}/4$) can be synthesised by 4 different converter states, two of them producing a positive slope on the circulating current (states $C_1$ and $C_2$) and two generating a negative slope on the circulating current (states $C_7$ and $C_{10}$). Also from Table I, there are 6 redundant converter states available to generate a zero output voltage (states $C_0$, $C_6$, $C_8$, $C_9$, $C_{11}$, and $C_{12}$). Two of them cause a large positive or a large negative circulating current slope (states $C_0$ and $C_{10}$), respectively, while for the other 4 redundant zero output voltage states the circulating current remains constant.

### III. Decoder Requirements for MMC Converters

Since PD-PWM does not select between the various converter redundant states shown in Table I, the switching command signals synthesised by this modulation scheme must be post-manipulated by a decoding structure. This can be done

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**TABLE I: EFFECT OF PHASE LEG SWITCHED STATES ON THE COMMON- AND DIFFERENTIAL-MODE QUANTITIES**

<table>
<thead>
<tr>
<th>C</th>
<th>$\sigma_1$</th>
<th>$\sigma_2$</th>
<th>$\sigma_3$</th>
<th>$\sigma_4$</th>
<th>$v_3$</th>
<th>$v_2$</th>
<th>$v_1$</th>
<th>$v_0$</th>
<th>$v_{lower}$</th>
<th>$v_{upper}$</th>
<th>Level</th>
<th>$v_{cm} - v_o$</th>
<th>$i_{cm}$</th>
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<tbody>
<tr>
<td>$C_0$</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>$V_{dc}/2$</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>$V_{dc}$</td>
<td>$L_4$</td>
<td>$V_{dc}/2$</td>
<td>$V_{dc}/2$</td>
</tr>
<tr>
<td>$C_1$</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>$V_{dc}/2$</td>
<td>$V_{dc}/2$</td>
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<td>0</td>
<td>$V_{dc}$</td>
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<td>$V_{dc}/4$</td>
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<td>$C_{10}$</td>
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<td>0</td>
<td>$V_{dc}/2$</td>
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<td>$V_{dc}$</td>
<td>$L_2$</td>
<td>$V_{dc}/2$</td>
<td>$V_{dc}/2$</td>
</tr>
</tbody>
</table>

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The table shows how the voltages on the common mode ($v_{cm}$) and differential mode ($v_{dm}$) are calculated based on the switch states. The voltages are calculated as follows:

- $v_{cm} = \frac{(v_{lower} + v_{upper})}{2}$
- $v_{dm} = v_0 - \frac{(v_{lower} - v_{upper})}{2}$

The table also includes columns for the resulting upper and lower arm voltages ($v_{upper}$ and $v_{lower}$) and the circulating current ($i_{cm}$).
by using a finite state machine decoder to equally distribute the switching events across all module semiconductor devices according to a given criterion [13]-[15]. In particular for the MMC topology, the decoder must additionally perform the function of controlling the converter phase leg dc level and high-frequency circulating currents.

The phase leg circulating current can be maintained at a constant dc bias level with minimum switching ripple by satisfying two essential requirements. Firstly, every time the modulator/decoder is required to produce the output voltage level $L_i$ (i.e. $v_o = V_{dc}/4$), this should be done on an alternating round-robin basis to select between the positive-$i_{cm}$-slope and negative-$i_{cm}$-slope redundant states, $\{C_4, C_5\}$ and $\{C_D, C_E\}$, respectively, i.e. following for example the pattern $C_4 \rightarrow C_D \rightarrow C_8 \rightarrow C_E$. Similarly, for synthesis of output voltage level $L_1$ (i.e. $v_o = -V_{dc}/4$), this should be done by alternatively selecting between redundant state sets $\{C_1, C_2\}$ and $\{C_7, C_B\}$, i.e. for example following the pattern $C_1 \rightarrow C_7 \rightarrow C_2 \rightarrow C_B$. Secondly, every time the modulator/decoder is commanded to produce the zero output voltage level $L_0$, this should be done by selecting on a round-robin basis the $i_{cm}$-constant redundant states $C_6$, $C_{10}$, $C_9$, and $C_A$, and avoiding the use of the two zero-output-voltage redundant states that produce the large positive/negative circulating current slopes (states $C_0$ and $C_F$).

IV. CONVENTIONAL (2N+1) FIVE-LEVEL PD-PWM DECODER

Fig. 2(a) and 2(b) show a (2N+1) five-level PD modulator with a finite state machine post modulator decoder that fulfils these requirements, built using the principles from [15]. The decoder inputs are the 4 PD-PWM logic switching signals $s_0$, $s_1$, $s_2$, and $s_3$, while the decoder outputs are the gate signals $\sigma_0$, $\sigma_1$, $\sigma_2$, and $\sigma_3$ which drive the individual module active upper switches (lower switches are driven in a complementary fashion with the inclusion of dead-time). The finite state machine contains 32 states and 56 transitions (self-loop transitions are omitted for clarity since they do not change the output action), and its present state depends on the past output voltage level transitions $L_i$, $i = \{0, 1, 2, 3, 4\}$.

Within a particular disposition band, this strategy produces a relatively well-behaved circulating current. However the current dc bias point does drift away during a band change transition, as shown in Fig. 2(c). This occurs because in PD-PWM the active switched pulse position is displaced by one half-carrier period when changing bands, and this causes the redundant state to become one-half carrier period shorter just after the band transition, as illustrated in Fig. 2(c). This circulating current dc bias drift is quite undesirable since it causes low-frequency oscillations on the individual module capacitor voltages.

V. OPTIMISED (2N+1) FIVE-LEVEL PD-PWM DECODER

Circulating current dc bias drifts can be compensated by applying an additional redundant state selection immediately after a band transition has occurred. This is illustrated in Fig. 3. Fig. 3(a) shows the conventional scenario with the shortened redundant state at the band transition, which leads to a decrease in the circulating current bias in the next redundant state (for example the highlighted $\sigma_1\sigma_2\sigma_3\sigma_0 = \{1101\}$ state shown on the left-side of Fig. 3(a)). However this effect can be avoided by forcing a further redundant state selection (for example the change of $\sigma_3\sigma_2\sigma_1\sigma_0$ from 1101 to 0100 shown on the left-side of Fig. 3(b)) midway through the first half-carrier interval after the band transition. This additional selection compensates for the shortened redundant state at the band transition, and drives the circulating current back to its original dc operating point.
Since the redundant state shortening interval is always one-half-carrier period, the timing for the additional redundant state selection should be set to be exactly midway through the half-carrier interval that follows a band transition. This is most conveniently achieved with an ancillary square wave signal \( s_q \), constructed by comparing a fixed modulation reference \( m_{m} = 0.75 \) against carrier \( c_0 \) as shown in Fig. 4(a). \( s_q \) is then fed to a finite state machine decoder built upon the principles of [15] but augmented to incorporate 24 additional states for managing the band transitioning process as shown in Fig. 4(b). The decoder inputs are the 4 PD-PWM logic switching signals \( s_0, s_1, s_2, \) and \( s_3 \) and the square wave signal \( s_q \), while the decoder outputs are the gate signals \( \sigma_0, \sigma_1, \sigma_2, \) and \( \sigma_3 \) which drive the individual MMC modules.

From Fig. 4(b), the circular path from states \( S_0 \) through to \( S_7 \) and back to \( S_0 \) defines the operation for Band 0. Similarly, circular paths from states \( S_8 \) to \( S_{15} \) back to \( S_8 \), \( S_{16} \) to \( S_{23} \) back to \( S_{16} \), and \( S_{24} \) to \( S_{31} \) back to \( S_{24} \) define the operation for Bands 1, 2, and 3, respectively. None of these paths depend on the square wave signal \( s_q \) and were conceived essentially to select the redundant states on a round-robin basis as per [15]. Paths from states \( S_{32} \) to \( S_{39} \), \( S_{36} \) to \( S_{37} \), \( S_{38} \) to \( S_{40} \), and \( S_{41} \) to \( S_{43} \) dictate the behaviour when moving from Band 0 to Band 1, and paths from states \( S_{44} \) to \( S_{46} \), \( S_{47} \) to \( S_{49} \), \( S_{49} \) to \( S_{52} \), and \( S_{53} \) to \( S_{55} \) define the behaviour when moving from Band 1 to Band 0. Both paths reverse the slope of the circulating current midway through the band transition event, using changes on the square wave signal \( s_q \) as a timing generator for the slope reversal. Similar paths manage the transitions from Bands 2 to
3 and vice-versa, however paths from Bands 1 to 2 and 2 to 1 do not incorporate additional states, since the band transitioning drift on the circulating current dc bias is very small for those band changes as shown in Fig. 3(b).

State machine decoders for MMCs with higher number of cells per arm can be developed following the same approach as exemplified in this paper for the particular case of two cells per arm. In general, for a MMC with N cells per arm, the decoder structure consists of 2N rows corresponding to each PWM disposition band, each with 4N logical states to account for the total number of phase leg sub-modules (i.e. 2N) and the two switching events produced within each carrier interval. Within this structure, sub-module switched states are then allocated to their relevant row for a given disposition band, in a sequence that balances the usage of upper and lower arm sub-module devices while simultaneously achieving cycle-by-cycle reversal of the common-mode voltage to constrain the circulating current. In addition, the decoder arrangement also contains 4N triplets of states for each disposition band to specifically constrain the common-mode current during a band change, except for the central disposition band where a direct transitioning between bands (i.e. without the circulating current slope reversal midway through the band transition event) causes minimal disturbance to the common-mode current.

VI. SIMPLIFICATION FOR \((N+1)\) THREE-LEVEL PD-PWM

Inspection of Table I indicates that for the set of switched states responsible for the synthesis of levels \(L_0\), \(L_2\), and \(L_4\), the common-mode current remains constant (except for the unused states \(C_0\) and \(C_F\)), whereas for the switching states that produce levels \(L_1\) and \(L_3\), the circulating current presents varied slopes according to the selected redundant state. Hence a much simpler decoder can be developed for implementing \((N+1)\) three-level PD-PWM for MMCs that readily produces a common-mode current free of high frequency components, by avoiding the use of switching states that produce levels \(L_1\) and \(L_3\). Fig. 5(a) shows the modulator/decoder structure, where two three-level PD logic switching signals \(s_{01}\) and \(s_{23}\), synthesised by comparing a sinusoidal reference \(m_0\) with two level-shifted carriers \(c_{01}\) and \(c_{23}\), are fed to a post modulator decoder to generate the 4 gate signals \(\sigma_0\), \(\sigma_1\), \(\sigma_2\), and \(\sigma_3\) which drive the individual modules. The finite state machine arrangement is shown Fig. 5(b), with resulting waveforms presented in Fig. 5(c), showing a constant circulating current at the dc bias level as expected.

In general, for a MMC with N cells per arm, the decoder structure has N rows corresponding to each PWM disposition band, each with 4N logical states to account for the total number of phase leg sub-modules (i.e. 2N) and the two switching events produced within each carrier interval. Within this structure, sub-module switched states are allocated to their relevant row for a given disposition band, in a sequence that balances usage of upper and lower arm sub-module devices.

VII. SIMULATION AND EXPERIMENTAL RESULTS

The concepts presented in this paper have been validated using detailed PSIM switching models, and a prototype N = 2 MMC phase leg with parameters as listed in Table II. A Texas Instruments TMS320F2812 processor was used for the PWM generation and the post modulation decoding schemes were implemented on an Altera MAX-II EPM570T100C5 CPLD.

<table>
<thead>
<tr>
<th>Table II: System Parameters</th>
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<tr>
<td>Description</td>
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<tr>
<td>Number of modules per arm</td>
</tr>
<tr>
<td>dc-link voltage</td>
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<tr>
<td>Fundamental frequency</td>
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<td>Individual module switching frequency</td>
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<td>Effective switching frequency</td>
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<td>Individual module bus capacitors</td>
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Fig. 6 presents simulation waveforms for the five-level PD MMC modulation with optimized post modulator decoding as per Fig. 4. More specifically, Fig. 6(a) shows the phase leg output voltage $v_o$ with the anticipated five distinct voltage levels (the slight level slope is caused by low frequency ripple in the sub-module dc-link voltages). Fig. 6(b) shows the upper and lower arm currents, $i_{\text{upper}}$ and $i_{\text{lower}}$, respectively, and Fig. 6(c) shows the resulting common-mode (circulating) current $i_{\text{cm}} = (i_{\text{upper}} + i_{\text{lower}})/2$ and differential-mode (output) current $i_{\text{dm}} = (i_{\text{upper}} - i_{\text{lower}})/2 = i_o/2$. From Fig. 6(c), the common-mode current $i_{\text{cm}}$ is well behaved and operates around a bias level (note that besides containing a dc component $I_{\text{cm}}$ it also has a low frequency oscillation as a consequence of sub-modules dc-link voltage ripple). Finally, Fig. 6(d) shows that the state machine decoder is able to achieve natural balancing of the module capacitor voltages ($v_{C0}$ through to $v_{C3}$) as desired.

Fig. 6: Simulation results for five-level PD-PWM decoder: (a) switched output voltage $v_o$, (b) arm currents $i_{\text{upper}}, i_{\text{lower}}$, (c) circulating current $i_{\text{cm}}$ and output current $i_o$, (d) individual module capacitor voltages $v_{C0}, v_{C1}, v_{C2}, v_{C3}$.

Fig. 7: Simulation results for three-level PD-PWM decoder: (a) switched output voltage $v_o$, (b) arm currents $i_{\text{upper}}, i_{\text{lower}}$, (c) circulating current $i_{\text{cm}}$ and output current $i_o$, (d) individual module capacitor voltages $v_{C0}, v_{C1}, v_{C2}, v_{C3}$.
Fig. 7 shows simulation plots for the MMC three-level PD-PWM with simplified decoder as per Fig. 5. In particular, Fig. 7(a) shows the phase leg switched output voltage $v_o$ (in this case with three definite voltage levels), Fig. 7(b) shows the upper and lower arm currents, $i_{upper}$ and $i_{lower}$, respectively, and Fig. 7(c) shows the circulating and output currents, $i_{cm}$ and $i_o$, respectively. From Fig. 7(c), the common-mode current $i_{cm}$ is now free of high frequency components and only contains the dc bias plus low frequency oscillation, while the output current $i_o$ presents higher ripple magnitude as expected. Fig. 7(d) shows that also for the simplified decoder, natural balancing of the module capacitor voltages is achieved.

Matching experimental results for the five-level optimized PD-PWM decoder and for the simplified three-level PD-PWM decoder, are presented in Figs. 8 and 9, respectively, confirming the practical viability of these two approaches. In addition, Figs. 10 and 11 present the simulated and experimental MMC phase voltage spectrum achieved with these two decoding techniques, which both clearly show the large dominant carrier harmonic expected for PD-PWM (which cancels in the line-to-line output voltage and hence reduces the overall inverter distortion). These results confirm that PWM of the overall MMC phase leg with a PD strategy and a per phase (instead of per arm) state machine post modulator decoder allows for the exploitation of the superior harmonic properties of the PD-PWM strategy.

VIII. CONCLUSION

This paper has discussed the design and implementation of per phase finite state machine PD-PWM post modulator decoders for modular multilevel converters. A methodology for developing optimised state machine decoders for MMCs that are capable of synthesising $2N+1$ switched phase leg output voltage levels while still maintaining balance of the individual module capacitor voltages has been presented through its application to a two module per arm MMC. A simplified version of MMC PD-PWM post modulator decoder, able of synthesising $N+1$ phase leg output switched voltage levels while also maintaining the individual module capacitor voltages balanced, has been introduced by its development to the same two module per arm MMC scenario.
Both of these methodologies have been extensively investigated using PSIM switched simulations and then experimentally confirmed using an exemplar MMC phase leg.

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