On Frequency Domain Analysis of Dual Active Bridge DC-DC Converters

A thesis submitted in fulfilment of the requirements for the degree of Doctor of Philosophy

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Kind regards, Jan Riedel
Declaration

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Jan Riedel
Stuttgart. March 18, 2017
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Publications

Conference Papers

Transaction Papers
Selected Patents

- METHOD AND SYSTEM FOR THE CONTACTLESS CHARGING OF A BATTERY-OPERATED OBJECT Veröffentlichungsnummer WO 2016055180 A1

- CONVERTERS AND METHODS FOR CONTROLLING A CONVERTER Aktenzeichen DE 102016208570.0

- METHODS FOR DETECTING A CONVERTER IMPEDANCE Aktenzeichen DE 180916184211.7
List of Symbols

**Stiff DC bus properties**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{p,DC}$</td>
<td>Half primary DC bus voltage</td>
</tr>
<tr>
<td>$V_{s,DC}$</td>
<td>Half secondary DC bus voltage</td>
</tr>
<tr>
<td>$d$</td>
<td>DC-DC bus voltage ratio (absolute or referred to primary)</td>
</tr>
<tr>
<td>$i_{p,DC}^0$</td>
<td>Mean primary DC bus current</td>
</tr>
<tr>
<td>$i_{s,DC}^0$</td>
<td>Mean secondary DC bus current</td>
</tr>
<tr>
<td>$P_{p,DC}$</td>
<td>Primary DC bus power</td>
</tr>
<tr>
<td>$P_{s,DC}$</td>
<td>Secondary DC bus power</td>
</tr>
</tbody>
</table>

**AC link properties**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n$</td>
<td>Harmonic counter for AC link quantitites ($n=1, 2, 3,... N$)</td>
</tr>
<tr>
<td>$m$</td>
<td>Harmonic order $m = [2n - 1]$</td>
</tr>
<tr>
<td>$N$</td>
<td>Maximum number of harmonics considered</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$v_p$</td>
<td>Primary bridge output voltage (time domain)</td>
</tr>
<tr>
<td>$V_p^m \angle \vartheta_p^m$</td>
<td>Primary bridge output voltage harmonic (frequency domain)</td>
</tr>
<tr>
<td>$v_s^{(\prime)}$</td>
<td>Secondary bridge output voltage (time domain)</td>
</tr>
<tr>
<td>$V_s^{(\prime)m} \angle \vartheta_s^m$</td>
<td>Secondary bridge output voltage harmonic (frequency domain)</td>
</tr>
<tr>
<td>$i_p$</td>
<td>Primary bridge output current (time domain)</td>
</tr>
<tr>
<td>$i_s^{(\prime)m} \angle \vartheta_s^m$</td>
<td>Secondary bridge output current (time domain)</td>
</tr>
<tr>
<td>$I_p^{(\prime)m} \angle \vartheta_p^m$</td>
<td>Primary bridge output current harmonic (frequency domain)</td>
</tr>
<tr>
<td>$I_s^{(\prime)m} \angle \vartheta_s^m$</td>
<td>Secondary bridge output voltage harmonic (frequency domain)</td>
</tr>
</tbody>
</table>

**AC link impedances**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$[Y]$</td>
<td>Admittance matrix of AC link coupling impedance</td>
</tr>
<tr>
<td>$Y_{s,x}$</td>
<td>Self or mutual admittance matrix elements</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{\sigma,p}$</td>
<td>Primary coil leakage inductance</td>
</tr>
<tr>
<td>$L'_{\sigma,s}$</td>
<td>Primary-side referred secondary coil leakage inductance</td>
</tr>
<tr>
<td>$L_m$</td>
<td>Primary-side referred magnetising (mutual) inductance</td>
</tr>
<tr>
<td>$R_{\sigma,p}$</td>
<td>Primary coil AC resistance</td>
</tr>
<tr>
<td>$R'_{\sigma,s}$</td>
<td>Primary-side referred secondary coil AC resistance</td>
</tr>
<tr>
<td>$N_p : N_s$</td>
<td>Transformer turns ratio</td>
</tr>
<tr>
<td>Symbol</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>$k_T, K$</td>
<td>Transformer coupling co-efficient, Modified coupling co-efficient</td>
</tr>
<tr>
<td>$\chi$</td>
<td>Transformer split leakage inductance</td>
</tr>
<tr>
<td>$L$</td>
<td>Inductance of coupled inductor</td>
</tr>
<tr>
<td>$R$</td>
<td>Resistance of coupled inductor</td>
</tr>
</tbody>
</table>

**DC bus properties**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l$</td>
<td>Harmonic counter for DC bus quantities ($l=1, 2, 3, ...$)</td>
</tr>
<tr>
<td>$k$</td>
<td>Harmonic order $k = [2l]$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_{p,DC}$</td>
<td>Primary DC bus current (time domain)</td>
</tr>
<tr>
<td>$i_{p,DC}^k \angle \theta_{p,DC}^k$</td>
<td>Primary DC bus current harmonic (frequency domain)</td>
</tr>
<tr>
<td>$i_{s,DC}$</td>
<td>Secondary DC bus current (time domain)</td>
</tr>
<tr>
<td>$i_{s,DC}^k \angle \theta_{s,DC}^k$</td>
<td>Secondary DC bus current harmonic (frequency domain)</td>
</tr>
<tr>
<td>$i_{cap}$</td>
<td>Primary DC bus capacitor current (time domain)</td>
</tr>
<tr>
<td>$i_{cap}^k \angle \theta_{cap}^k$</td>
<td>Primary DC bus capacitor current harmonic (frequency domain)</td>
</tr>
<tr>
<td>$i_{src}$</td>
<td>Primary DC bus source current (time domain)</td>
</tr>
<tr>
<td>$i_{src}^k \angle \theta_{src}^k$</td>
<td>Primary DC bus source current harmonic (frequency domain)</td>
</tr>
</tbody>
</table>

**DC bus impedances**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{DC}$</td>
<td>Primary bridge DC bus capacitance</td>
</tr>
<tr>
<td>$R_{ESR}$</td>
<td>Equivalent series resistance of DC bus capacitor</td>
</tr>
<tr>
<td>$L_{DC}$</td>
<td>DC bus line inductance</td>
</tr>
<tr>
<td>$R_{DC}$</td>
<td>DC bus line resistance</td>
</tr>
</tbody>
</table>

**Practical switching impact**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta i_p$</td>
<td>Min. ZVS circulating current (primary bridge)</td>
</tr>
<tr>
<td>$\Delta i_s$</td>
<td>Min. ZVS circulating current (secondary bridge)</td>
</tr>
<tr>
<td>$\rho_{DT_p}$</td>
<td>Dead-time angle (primary bridge)</td>
</tr>
<tr>
<td>$\rho_{DT_s}$</td>
<td>Dead-time angle (secondary bridge)</td>
</tr>
</tbody>
</table>

**Modulation control angles**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\delta$</td>
<td>Phase shift between primary and secondary bridge</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>Primary bridge duty cycle (single phase DAB)</td>
</tr>
<tr>
<td>$\beta$</td>
<td>Secondary bridge duty cycle (single phase DAB)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\nu_{s,z}$</td>
<td>Compensation angles (three-phase DAB)</td>
</tr>
</tbody>
</table>

**Miscellaneous**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$w_{sw} = 2\pi f_{sw}$</td>
<td>Fundamental angular switching frequency (in rad/s)</td>
</tr>
<tr>
<td>$f_{sw} = 1/T_{sw}$</td>
<td>Fundamental switching frequency ($T_{sw}$: switching period)</td>
</tr>
</tbody>
</table>
Abstract

Modern society uses electrical energy for a wide range of needs and requirements. Electrical energy is considered high value as it requires a prior conversion step from kinetic/thermal or solar energy. However, electrical power is always defined by certain properties which typically need to be adjusted in multiple stages to satisfy the specifications of electrical loads such as motors, lighting and consumer electronics. For DC (direct current) power systems, switching DC-DC power converters are the state-of-the-art solution to achieve a low-loss modification of the voltage magnitude.

The Dual Active Bridge (DAB) converter is an attractive DC-DC conversion topology that can widely satisfy the future needs of DC power management and the integration of electro-chemical storage. It offers an unmatched capability to transfer energy in either direction between two DC sources while its inherent Zero Voltage Switching capability offers potential for high conversion efficiency and high power density.

The current and future research activities on DAB converters mainly focus on maximising the power density through a volume reduction of the embedded passive power devices. This trend is encouraged by the market introduction of wide bandgap fast-switching semiconductor devices using Silicon Carbide (SiC) and Gallium-Nitride (GaN) to replace conventional Silicon material in many applications. The reduced parasitic capacitance and transition time of these devices allow to significantly increase the converter operating frequencies, which is the only way to increase the power density unless the material specifications of passive power devices drastically evolve. However, a higher operating frequency inevitably leads to a stronger influence of practical second-order effects, which for a DAB, particularly address the non-ideality of the switch devices, the parasitic coupling impedances in the high-frequency transformer, the peripheral connecting traces of the AC link network and the DC bus filter. Hence, all these effects have to be accommodated by a universal design framework which is yet to be found in literature.

A DAB is conventionally designed using time domain analysis of the modulation sequence and device waveforms to evaluate its key performance design criteria such as active power transfer, Zero Voltage Switching (ZVS) and AC link circulating power. This analysis technique typically presumes an idealized single parameter AC link inductance to substitute for the more complex circuit model of a practical high-frequency transformer. This becomes particularly relevant as the operating frequencies increase, causing both active and passive power devices to become less ideal. More than that, advanced multi-level
DAB Phase Shifted Square Wave (PSSW) modulation strategies lead to a wide solution space of control parameters that can be used to enhance the performance of a DAB by shaping the AC link current in certain ways. Within the time domain, such volatile modulation strategies require a complicated structure model analysis.

This thesis now shows how to apply frequency domain harmonic analysis techniques to a DAB DC-DC converter. The approach readily accommodates the influence of complex impedance structures, practical switching effects and advanced multi-level modulation concepts, and leads to generic numerical and analytical solution expressions that significantly enhance the converter design process. The work thus establishes a new analysis strategy in the advancing field of DAB research.

The thesis begins with the harmonic decomposition of the bridge output voltages and the expression of the DAB coupling network as a generic two-port impedance model. These steps establish the frequency domain analysis (FDA) framework.

Next, the FDA approach is applied to derive explicit solution terms for the ZVS regions of single and three-phase DAB converters, which are crucial to minimise the power loss of the semiconductor devices during the switching transition. These expressions are used to separately investigate the impact of single impedance parameters, non-ideal switching transitions and PSSW modulation concepts on the ZVS limiting conditions, which determine the preferable operating regions to achieve minimum switching loss operation and best possible controllability of the DAB. From this work, it is shown how a single element high-frequency transformer with a reduced coupling factor is sufficient to ensure continuous and reliable ZVS operation without adding software or auxiliary hardware complexity. More than that, the strategy quantifies the impedance design parameters of the coupling network in correlation with the selected PSSW modulation concept. In this context, the benefit of adaptive 3-level DAB modulation is presented to support continuous ZVS operation and thus allow for high-efficient operation of a single phase DAB across its entire operating range.

Finally, the established modeling framework is extended to identify the DC bus harmonics injected by the PSSW modulation process, for any particular DAB design and operating context. It is also shown how adaptive modulation can be used to mitigate certain harmonic frequencies that can otherwise cause severe harmonic interferences, DC bus oscillations, and thus impact on the DC side filter design process.

To complete the work, experimental results are presented to verify the analytical development, using a laboratory DAB converter that can operate across a wide range of DC voltages at power levels up to 1 kW. Simultaneously, as part of an industry project with BOSCH, a customised 1.2 kW DAB prototype was built using the presented design guidelines, which achieved a conversion efficiency between 96.5% and 98.5% across the operating range.
1 Introduction

1.1 Background

The majority of global power distribution uses AC (alternating current) to transfer energy between the generation and the load. This technology approach is well-known to facilitate circuit interruption and voltage conversion using high-power 50/60 Hz transformers. However recently, more and more electrical energy is consumed or generated as DC (direct current) power, such as LED lighting, consumer electronics and a majority of renewable power sources. Large-scale (e.g. offshore high-voltage DC grids) and small-scale (e.g. local generation, buildings or electric vehicles) DC power transmission is encouraged to minimise the number of conversion stages and thus increase the investment benefit and the transmission efficiency. As a result, the proportion of DC-based power transmission and distribution is expected to increase in the future, which reduces the overall energy loss created due to the conversion of electrical power.

Electro-chemical battery storage technology offers a way to maximise the integration of renewable power sources, with local on-site generation and storage systems implemented to minimise the grid loading and the average transmission distance. Indeed, this support is necessary to maintain the power and voltage quality of the co-existent AC grid. Unfortunately, the DC output voltage of each energy storage galvanic cell is only a few volts, and the number of cells that can be connected in series inside a battery pack is typically limited by performance and safety considerations. This creates a need for highly-efficient step-up bi-directional DC-DC converters, to transfer power between these batteries and a higher voltage magnitude access point.

DC-DC switch power converters are traditionally classified into two groups: isolated and non-isolated topologies. Generally they are based around a phase leg which combines a low-side and a high-side switch device to create an alternating output voltage pattern across an inductive storage element. A combination of two or three phase legs establishes a single phase or three-phase bridge. If a galvanic isolation or a large step-up ratio between the two DC ports is required, a transformer can be integrated between two such converter bridges. These isolated converter topologies are typically operated using Phase Shifted Square Wave (PSSW) Modulation rather than Pulse Width Modulation (PWM) control. Each phase leg (and hence each switch device) is typically switched with 50% duty cycle square waves, while the switching transition of each phase leg can be delayed with respect to one another to control
1.2 AIMS OF THE RESEARCH

The common strategy of applying time domain analysis to a DAB limits the design context to an idealised series impedance connected between the two bridges. This becomes increasingly restrictive as the operating frequencies increase and both active and passive power components become less ideal. Furthermore, apart from the inevitable approximation errors caused by this approach, the reduction of the modeling complexity suppresses potential design or modulation opportunities of benefit. In addition, the use of a more advanced PSSW modulation pattern further complicates the time domain analysis approach, making it unable to establish a universal design and analysis platform that can comprehensively evaluate key DAB performance criteria such as the active power transfer, Zero Voltage
Switching (ZVS) and AC link circulating power. And finally, apart from these limitations with the AC link analysis, the time domain analysis approach almost invariably cannot widely quantify the DC bus current, which is however necessary for effective DC side filter design.

Hence, this thesis now aims to establish a powerful mechanism for AC link and DC bus analysis of DAB converters that readily accounts for any AC link impedance variation, more advanced modulation strategies and the most dominant second order effects. In particular, the approach can accurately and broadly determine the ZVS boundaries and power transfer relationship of a DAB under all operating and impedance conditions, while also incorporating the use of adaptive DAB modulation concepts and accommodating the practical switching effects of phase leg dead-time delay and parasitic device capacitance. The analysis approach thus allows to best utilise the design and control freedoms offered by a DAB for any particular application context.

1.3 Structure of Thesis

The thesis is presented in ten chapters. In the first two chapters the broader research context is outlined and prior literature on DAB converters is reviewed. Chapters 3-8 contain the major original contributions of this work and guide the reader through the frequency domain analysis strategy which is used to derive general DAB design guidelines. Chapter 9 provides a brief summary of the simulation and experimental systems, while Chapter 10 concludes the thesis.

Chapter 1 (this Chapter) provides the broad research context, which is followed by the original contribution identified in this thesis.

Chapter 2 presents the literature review. It summarises the existing range of research publications in the field of DAB converters, and then identifies their limitations when used with higher order complex impedance models and advanced modulation strategies.

Chapters 3 and 4 present the new approach to determine the ZVS boundary conditions of a single and three-phase DAB using harmonic decomposition of the bridge switching patterns and a two-port network analysis. This gives an explicit theoretical solution under all operating conditions, while also accommodating more complex AC link impedance structures, practical impedance non-idealities, and the switching impact of dead-time and device capacitance. The effects of these practicalities and adaptive modulation concepts on the ZVS region are individually explored. For a three-phase DAB, the possibility of an asymmetric modulation pattern is investigated to extend the available ZVS region for an unbalanced three-phase transformer impedance. The analytical predictions are confirmed by matching analytical predictions with experimental results for selected DAB systems.

Following the conventional design target of maximising the transformer magnetising inductance to achieve lowest possible circulating current, non-ideal switching invariably leads to hard switching operation at particular operating conditions. To resolve this limitation, Chapters 5 and 6 introduce an analysis approach which can quantify the specific value of magnetising inductance that creates
just sufficient additional AC link circulating current to achieve continuous ZVS operation over the entire specified dc-dc voltage and power operating range of the converter without requiring additional components. The last section of this chapter presents an alternative DAB design approach by introducing a constrained ZVS operation that can be used to reduce the ZVS commutation loss in high-boost DAB converters caused by the parasitic commutation inductance, despite operating under ZVS conditions. The capability of the theoretical analysis process is confirmed by matching experimental results.

**Chapters 7 and 8** extend the harmonic analysis framework to include the DC bus harmonic currents that are created by a single or three-phase DAB for any operation or design context. In particular it shows how specific DC bus current harmonics can be actively suppressed using adaptive 3-level modulation as part of the filter design process. This particularly addresses a potential design difficulty of parasitic connection impedances that can cause hazardous DC bus oscillations. This new active harmonic suppression (AHS) strategy is validated by theory, simulation and matching experimental results.

**Chapter 9** describes the simulation and experimental test environments.

**Chapter 10** concludes the thesis and outlines some ideas for further work arising from the findings presented here.

### 1.4 Identification of Original Contribution

This thesis establishes a new analysis and design strategy for Dual Active Bridge (DAB) DC-DC converters. It overcomes the limitations of prior approaches by creating a widely applicable solution approach that gives guidance on how to design and operate a DAB to achieve the desired performance for any particular application context. There are three major and original contributions arising from this work.

The first contribution is to introduce and experimentally verify a new frequency domain analysis that detects the ZVS boundary conditions for any design and operating context of single and three-phase DAB converters. The basic principle is a generalised two-port AC link impedance model, which is analysed...
using superimposed individual AC link harmonic components of voltages and currents. This process is illustrated in Fig. 1.2 for two exemplar phase-shifted square wave (PSSW) bridge output voltage patterns at different voltage magnitudes. Derived from that, complex impedance models, non-idealities and asymmetries are gradually included into the analysis to investigate their individual influence on the DAB performance.

The second contribution is to use this new modeling framework to achieve an enhanced DAB converter design process. The ZVS boundary analysis is able to quantify the exact requirements for the HF transformer and the PSSW modulation concept to ensure continuous ZVS operation with minimum RMS circulating currents. This leads to a single customised component solution which increases the DAB power density and helps to keep the efficiency as high as possible throughout the entire operating range. For large boost ratio converters it is shown how the hard turn-off commutation loss can be minimised as a consequence of the transformer design process. For a three-phase converter in particular, the ZVS boundary analysis approach allows to adjust the six-step modulation pattern to account for the practical unbalance in high power density three-phase transformers that otherwise appear to reduce the ZVS operating range.

The third major contribution is the analytical determination of the DC bus harmonics of a single and three-phase DAB as an extension of the prior AC link analysis, which allows a more efficient filter design process. Beyond this, adaptive 3-level DAB bridge modulation is shown to be a way to mitigate certain harmonic frequencies that would otherwise be injected into the DC bus filter network and require to be passively damped by a large bus filter capacitor and/or inductor.
1.4. IDENTIFICATION OF ORIGINAL CONTRIBUTION
2 Literature Review on Dual Active Bridge (DAB) DC-DC Converters

This chapter presents a general overview of the reported literature on Dual Active Bridge DC-DC converters. More detailed literature review material is then incorporated into specific individual chapters of thesis as appropriate to the material considered in these chapters.

The Dual Active Bridge (DAB) is the ultimate choice for DC-DC converter applications where galvanic isolation and bi-directional power flow is required, the voltage boost ratio is too large for a non-isolated DC-DC converter and/or the power rating exceeds the feasibility of a reduced switch count flyback-type converter topology [3] [4]. Fig. 2.1 shows how the DAB can be used as a bi-directional charger for energy storage systems (fuel cell, battery, super-capacitors, etc.) [5] [6]. If a load is occasionally connected to the energy storage as is the case for battery-fed electrical drive powertrains, the DAB can also be an attractive solution for uni-directional power flow applications.

As energy storage becomes more commonplace in many industrial and automotive applications, the need increases for high-power converters to charge their high-energy storage systems within a reasonable period of time. For example, Fig. 2.2 shows the power system architecture of an electric vehicle (EV) as discussed in [7], where the embedded DAB allows to transfer power efficiently between the 13.5 V low voltage (LV) lead-acid battery and the 400 V high voltage (HV) lithium-ion traction battery. Furthermore, and compared to uni-directional isolated DC-DC converters, the DAB allows energy exchange in either direction, which may be required for safety reasons in case of failure of the traction battery, or to generally increase the freedom for in-vehicle power flow management. Other typical DAB applications have been considered in combination with renewable power sources (wind, solar), in small micro-grid architectures [8] - [11], in automotive on-board chargers [12] - [17], in aircrafts [18], on shipboards [19], in high-power AC-AC solid state transformers [20] [21] [22] and MVDC/HVDC grid power converter systems [23] [24].

Figure 2.1: DAB as bi- or uni-directional charger for energy storage systems
2.1 Fundamentals of DAB and Early Publications

The concept of a DAB DC-DC converter was first published in 1991 [1] titled as “A Three-phase Soft-Switched High-Power-Density dc/dc Converter for High-Power Applications”. This initial publication is the first major reference on DAB converters and describes the fundamental operating principles of this topology. Hence selected concepts from this work are now described in this first part of the literature review to summarise the basic operating principles of a DAB.

The publication proposed to utilise an intermediate single or three-phase AC coupling transformer between two active converter bridges to transfer energy between their respective DC ports in either direction. Each DC port is connected to a regular H-bridge (in case of a single phase DAB) or three-phase bridge (in case of a three-phase DAB), while the phase legs of each bridge are switched with 50% duty cycle square waves. For a single phase DAB, these are typically displaced exactly 180° out of phase (120° for the three-phase topology) to create a symmetrical AC square wave output. The two bridge voltage outputs are then displaced by a phase angle as single degree of control variable to regulate the power transfer. Fig. 2.3 shows the conventional single and three-phase DAB circuit topology with an intermediate high-frequency (HF) transformer.

While this primary DAB paper describes both the single phase and the three-phase DAB topology, it argues that the three-phase DAB topology leads to reduced AC link RMS and turn-OFF peak currents in the bridge switching devices, compared to its single phase equivalent. It also comments that the high-frequency six-step modulation of a three-phase DAB generates a high-frequency DC bus current waveform which reduces the DC bus filter requirements. This seminal paper uses time domain analysis to identify the key design criteria for a single phase and a three-phase DAB topology. It presumes a lossless transformer model with infinite magnetising inductance, which reduces the AC link impedance network down to the (inherent) total transformer leakage inductance. Piece-wise linear time domain
analysis is then used to analyse the system, recognising that the bridge modulators generate a four-step (single phase DAB) or twelve-step (three-phase DAB) AC voltage pattern across the leakage inductance $L$. The AC link current waveform is thus derived using the differential current equation of $\frac{dv_L}{dt} = \frac{v_1 - v_2}{L}$ where $v_L = v_1 - v_2$. Fig. 2.4 shows the resulting waveforms for the example of a single phase DAB including the respective DC bus currents, where it can be seen how one fundamental switching period comprises four segments with a separate current slope definition for each of them. The steady state periodicity is then used to develop a closed form analytical solution of the AC link current waveform. The average DC bus current allows to define the power transfer between the two DC outputs, which for an idealised single phase DAB with a single element series AC link inductance $L$ is as follows:

$$P_{p,DC} = \frac{d(2V_{p,DC})^2}{w_{sw} L} \delta \left(1 - \frac{|\delta|}{\pi}\right) \quad (2.1)$$

where $d$ is the DC-DC bus voltage ratio, $\delta$ is the phase shift angle (also: load angle) between the primary and the secondary side, and $w_{sw}$ is the angular switching frequency. Note also that for the three-phase topology analysis given in [1], the process shown in Fig. 2.4 needs to be applied (at least) twice as the switching sequence changes at a phase shift angle of $60^\circ$, which leads to two separate power equations and pairs of ZVS boundary conditions.

Ref. [1] also identifies that this DC-DC converter topology is capable of inherent Zero Voltage Switching (ZVS) under certain operating conditions. The ZVS switching boundary conditions for the primary and secondary converter bridge are derived by evaluating the AC link current polarity at the individual phase leg switching instances over time. The ZVS boundary operating conditions for the
idealised single phase DAB can be expressed as a relationship between the DC-DC bus voltage ratio $d$ and the phase shift angle $\delta$, for the primary bridge ($d_{ZVS_p}$) and the secondary bridge ($d_{ZVS_s}$), to be

$$d_{ZVS_p} \leq \frac{1}{1 - \frac{2|\delta|}{\pi}} \quad d_{ZVS_s} \geq 1 - \frac{2|\delta|}{\pi} \quad (2.2)$$

Both the power equation (2.1) and the ZVS boundary conditions (2.2) have become essential design and control guidelines since their initial publication, and are widely used in DAB literature.

Finally, this primary DAB publication also used AC phasors to model and characterise the DAB AC link network, defining the fundamental AC link harmonic voltage component of each bridge output to determine the voltage/current phasor across/inside the AC link inductance. This method is particularly identified as useful to evaluate the kVA rating of the transformer. An exemplar phasor diagram is sketched in Fig. 2.9 to illustrate this concept.

### 2.2 Successive DAB Publications

The attractiveness of an isolated DAB DC-DC converter to inherently achieve bi-directional power flow, galvanic isolation, Zero Voltage Switching (ZVS) and the integration of a variable voltage ratio transformer, has led to intense research activities in this area across the recent decades. It is commonly agreed that the DAB should operate as much as possible using Zero Voltage Switching (ZVS) to minimise...
device switching losses, particularly as converter switching frequencies increase with fast-switching wide bandgap semiconductor devices [25] - [29] entering the market. ZVS soft switching is shown to be crucial for these devices to achieve high-efficiency operation in the higher frequency range up to 1 MHz [30] [31] [32].

More recently, several papers have presented experimental proof of achieving high conversion efficiencies using the benefit of ZVS in conjunction with the progress of semiconductor device technology. For example, in 2015, a peak efficiency of 98.7% at 42% load condition was obtained for a 100 kW, 750 V DAB operated at 20 kHz using SiC-MOSFET/SBD Dual Modules [2]. In comparison, in 1991, for a 50 kW, 1.2 kV DAB power system operated at 50 kHz using silicon IGBTs, the peak efficiency was reported to be around 91% [33]. The research activities on DAB converters can be grouped into the following three areas:

- Modulation Strategies
- Optimisation of Magnetic Power Devices
- Modeling of DAB Non-Idealities

Recent research in each of these areas will now be reviewed in more detail.

2.2.1 Modulation Strategies

Fundamentals

Fig. 2.3 presented the conventional single phase DAB. The circuit topology comprises two opposing (primary and secondary) full bridge converters that are interlinked via an AC coupling impedance. Hence, there are four phase legs, each of which integrates a high-side and a low-side switch device. If there is no inherent body or monolithic anti-parallel diode integrated with the forward conducting active switch element, an external diode needs to be added.

Each phase leg is typically switched with 50% duty cycle square waves, i.e. the turn-ON (turn-OFF) instant of the low-side device follows the high-side turn-ON (turn-OFF) instant of the respective high-side device by half a switching period, and vice versa. This is referred to as Phase Shifted Square Wave (PSSW) modulation as is exemplarily illustrated in Fig. 2.5(a). Each of the four DAB phase leg switching transitions can be delayed over time with respect to one another. This results in three independent modulation degrees of freedom. These control angles can now be used to adjust the bridge output volt-seconds applied across the AC link network with the ability to shape the AC link current in certain ways.

Progression of DAB Modulation Strategies

Numerous approaches that utilise these three fundamental control degrees of freedom have been proposed in recent years. Ref. [34] [35] first explored the benefit of an extended ZVS range using a “novel pulse
width modulation strategy” by no longer constraining the two individual phase legs of one of the two bridges to be displaced by 180°, while maintaining the phase shift variation between the two bridges. This modulation concept creates two control angles as shown in Fig. 2.5(b). The introduction of this second control angle requires the distinction of operating modes as the switching sequence is analysed using piece-wise linear analysis. The reference work shows that modifying the bridge output voltage duty cycle helps to achieve complete ZVS operation of the DAB as the DC bus voltage magnitudes vary. The “Dual Phase Shift” (DPS) control in [36] then shows how this progression in modulation can further be used to reduce the (reactive power) circulating currents in the AC link of the DAB, which ultimately minimises the conduction losses in the switch devices and the HF coupling transformer or any other embedded power device.

The “New Modulation Strategy” (NMS) [37] and the “Triple Phase Shift” (TPS) control [38] then accommodate all possible three control angles into their modulation concept as shown in Fig. 2.5(c). For both concepts, the analysis of the AC link current waveform leads to an identification of the four most common operating modes.

In [7] and [39] the identification is further extended to its theoretical limit of twelve modes, which

![Diagram](image-url)
Figure 2.6: Eight switching sequences for 3-level/3-level modulated single phase DAB

are separately evaluated to determine their individual suitability in terms of switching condition and
RMS circulating current across the entire range of DC bus voltages and power transfer. In most cases
however, a distinction of two modes, referred to as “triangular” and “trapezoidal” modes according to
the shape of the resulting transformer current waveform, is regarded as sufficient to cover a large amount
of operating conditions, which helps to reduce the analysis complexity.

The three fundamental modulation concepts are summarised in Fig. 2.5. Note that the captions
express the most frequent terms used in literature, while the expressions in brackets represent the
respective terms used in this thesis. Similar modulation concepts to extend the ZVS region and reduce
the RMS current by utilising all three available control angles are proposed in [40] - [49], while the
fundamental principles remain. For illustration purposes, Fig. 2.6 sketches eight examplar switching
sequences for a 3-level/3-level modulated DAB.

A first attempt to overcome this distinction of cases by applying superposition principles for such
advanced modulation techniques is discussed in [50] using “generalized modeling and optimization of a
bidirectional dual active bridge dc-dc converter including frequency variation”. This work on combining
phase shift and variable frequency modulation considers the two phase legs of each bridge as independent
voltage sources that can be superimposed to develop a more generic power transfer model. This strategy
allows to avoid a complicated multi-modal operating analysis.
2.2.2 Optimisation of Magnetic Power Devices

The technical performance of a DAB converter is typically ranked by volume and efficiency objectives. The AC coupling impedance defines the AC link current waveform which is distinctive for the power transfer, the bridge switching conditions and the amount of circulating (reactive) power. Thus, research has particularly focused on modeling and optimising the AC coupling network to improve the DAB performance. At the same time, there is a trend to use very high operating frequencies, e.g. 1 MHz [51], and planar transformer technology [52] [53] to further reduce the volume of the magnetic power devices.

Optimisation of AC Link Series Inductance

The operation and control of a DAB highly depends on the high-frequency (HF) transformer impedance design between the two bridges being crucial for the converter performance. Literature particularly refers to the optimal design value of the total transformer leakage inductance (for a single component AC link network solution) or an additional external AC link inductor. Analytical approximation formulas to determine the leakage inductance for various physical coil and core geometries are presented in [54]. In [55] the best compromise value of leakage inductance to achieve ZVS operation and minimum circulating current in a three-phase DAB is determined to be a function of the specified DC-DC voltage operating range. This range typically centres about the unity DC-DC bus voltage ratio ($d=1$) as indicated by the rectangular section in Fig. 2.7.

The circulating RMS current through the transformer is also shown to reduce with a higher series inductance as the DC-DC bus voltage ratio boundaries deviate further away from unity. However, there is an upper limit for the leakage inductance value due to the maximum power transfer requirement that still needs to be satisfied by the design. A similar optimisation is conducted in [56] where a dominant external inductor is added in series to the HF transformer. Ref. [57] evaluates the design efforts for such a combined solution approach to effectively enhance the DAB performance for a wide operating range. As operating conditions vary, Ref. [58] suggests to use a flexible “dual leakage transformer” where an extra switch is integrated to adjust the leakage inductance between two discrete values and

![Figure 2.7: Specified voltage operating range around the unity DC-DC bus ratio](image)
select the value that creates the more beneficial AC link current waveform load-dependent. A higher inductance value is preferred during low load operation to comply with the ZVS boundary conditions from (2.2), while the lower value is used at higher power levels. In addition, instead of compensating a non-unity DC-DC bus voltage ratio by adapting the bridge output voltage over time, as shown in Fig. 2.5, a variable turns ratio transformer (using an electrical tap changer) can be implemented to adjust the effective DC-DC bus voltage ratio [59]. In [60] and [61] the monotonic AC link impedance network is extended by additional inductors connected across the bridge output terminals to allow for additional circulating magnetising current. Such an AC link circuit extension is then shown to maintain ZVS across a wider operating range despite parasitic switch device capacitance that needs to be fully discharged before the incoming device is turned ON.

**Power Dissipation in the Magnetics**

In order to estimate the power loss of the HF transformer (or the external series inductor) in a DAB, simplified analytical models have been developed and validated in the literature. These models can then be used to replace finite element analysis if their modeling accuracy is sufficient.

In general, the magnetic components dissipate power in both the core body and the copper windings. With respect to the core losses, the Improved Generalised Steinmetz Equation (IGSE) [62] is typically proposed to account for the non-sinusoidal AC link current waveform obtained for a conventional monotonic coupling impedance network. The performance of various core materials can be investigated using material-specific Steinmetz parameterisation to match the experimental observations [63] - [66].

The AC copper resistance of the magnetic power devices is known to significantly vary with the applied operating frequencies. As a consequence, literature has developed advanced analytical models to improve the accuracy in the expected conduction loss power dissipation [67] - [71]. The frequency dependencies of the DAB AC coupling impedances may significantly impact on the converter operating conditions and hence need to be included into the DAB modeling process. Other such DAB non-idealities are addressed in Section 2.2.3

**Variations of the Monotonic DAB Impedance Network**

The performance of a conventional DAB using monotonic AC coupling impedance elements, i.e. a HF transformer with optional series inductor as presented in Fig. 2.8(a) and 2.8(b), is compared to resonant tank impedance networks in [72] [73] [74]. In [75], it is described how the integration of a series resonant capacitor according to Fig. 2.8(c) negatively impacts the DAB power density and ZVS range, while the sinusoidal AC current shape can be beneficial to reduce the winding loss and the ZVS turn-off current magnitude. A LCL tank impedance network (Fig. 2.8(d)) is proposed in [76]. Many other such resonant impedance variations are proposed in literature.

Typically, such resonant converters are analyzed using fundamental AC phasor theory, which may provide sufficient model accuracy if frequency variation (i.e. quasi-resonant operation) or 3-level bridge
modulation concepts are not taken into account. Note also that there is a large number of overlapping publications from the field of bi-directional (wireless) inductive power transfer applications [77] [78] [79] [80] where the conventional high coupling factor DAB transformer is replaced by two loosely coupled sender and receiver coils.

2.2.3 Modeling of DAB Non-Idealities

Practical DAB impedance non-idealities and modulation dead-time have been identified to be of significant relevance [81] during the modeling process. Hence, prior literature has developed state-space and AC phasor analysis strategies to accommodate these non-idealities.

State-Space Modeling

A detailed small-signal state-space and full-averaging model of a phase shifted single phase DAB converter with intermediate AC link inductance and DC bus filter is developed in [82] [83]. The modeling approach includes the DC bus filter time constant on either side of the DAB, which is found to be highly relevant to achieve effective closed loop voltage and power control of a DAB. The authors also mention that a precise knowledge of the PSSW modulation technique is mandatory for dynamic modeling and effective design of the digital controller (note that the Lyapunov function method in [84] confirms the general stability of a DAB disrespective of the selected PSSW modulation technique). Alternating analysis methods have been widely reported: In [85], an extended sixth-order DAB small-signal model is presented while reduced order DAB state-space models are developed in [86] and [87]. Further small signal steady-state and transient modeling strategies have been reported [88] [89]. The traditional volt-

![Diagram](image-url)

Figure 2.8: Typical AC link coupling networks of DAB converters
age control loop design method can be extended by adding inverse model-based feedforward terms in parallel to the PI voltage controller output, which calculate the required phase shift angle to immediately push the DAB to the target operating condition [90]. This is shown to improve the response time.

A similar state-space and average modeling technique is proposed for a three-phase DAB [91]. Further work to improve the dynamic response of a three-phase DAB has been published [92] [93] [94], where an instantaneous 2D stationary frame is used to limit the AC link peak current and thus avoid a DC bus current overshoot. Another dynamic modulation technique to avoid DC bus current overshoot for a single phase DAB is described in [95]. Simple steady-state analysis of the AC link current waveform is used to instantaneously calculate the DAB switching instants required subsequent to a load or voltage disturbance.

**AC Phasor Modeling**

Another approach to model a DAB is described in [91]. The fundamental phasor analysis in Fig. 2.9 is used to create a “first harmonic approximation” (FHA) of the AC link. In addition, the AC link current is translated into its respective average DC bus current to accommodate a linear DAB output load. A comparison to the previously discussed state-space modeling approach shows that there is a decent match with regards to the control response. However, the FHA approach is shown to have a significant deviation in the gain, which is traced back to the lack of higher-order harmonics that considerably contribute to the power transfer. Another deviation in the control response occurs due to the elimination of the transformer time constant in the state-space average model which is however obtained in the FHA model.

The FHA approach is then extended to a full-order harmonic summation in [96] [97] by segregating the primary and secondary bridge square wave output voltages into infinite odd frequency components. The solution terms can be used to predict the DAB phase shift control command. Beyond that, the nonlinear impact of dead-time is explored and is found to cause a significant error in the phase shift angle, i.e. a time delay in the actual voltage transition, as soon as hard switching occurs in either primary or secondary bridge. This leads to a deviated operating condition where the expected boundary conditions and the transferred power may substantially differ from the expected values. A compensation technique using a complicated distinction of operating modes is proposed, as is similarly done in [98] [99]. Both [91] and [96] show that frequency domain analysis can be used to comfortably accommodate the effect of AC
2.3 Issues in the Literature and Conclusion

The literature review has shown how various research groups have extended the fundamental modeling strategy from [1] to account for non-idealities, advanced modulation strategies or DAB circuit variants. In particular, the progression from conventional single phase shift (i.e. 2-level) modulation to triple phase shift (i.e. 3-level) modulation achieves a significant voltage range extension at the cost of slightly increased modulation resources. Furthermore, prior research has realised that switching dead-time, parasitic device capacitance, transformer resistance and such other second order effects can greatly influence the switching conditions and the power transfer of a DAB. Also, numerous variations of the bridge circuits and the AC link impedances have been investigated to achieve best possible performance for each individual application context.

At the same time, one can identify that the presented analysis strategies prevent the emergence of more generic design and modulation guidelines. This seems to be caused by the fact that, firstly, most records in the literature use conventional time domain analysis to model the DAB. As shown by the literature review, this approach almost inevitably limits the design scope to an idealised impedance structure. In most cases, the transformer impact can only be approximated but more significantly, the actual transformer design scope is based on the presumption of a fixed or variable [101] single-parameter AC link inductance optimisation which typically aims to achieve ZVS conditions for particular load conditions. The design strategies proposed in the literature are generally not able to take into account higher-order and non-linear coupling impedance models.

Secondly, numerous research papers have proposed adaptive 3-level DAB phase shift modulation strategies to achieve a flexible volt-second bridge output. These techniques essentially utilise the same three control degrees of freedom (if combined frequency variation [50] [102] [103] and burst mode operation [104] are not included) to extend the ZVS range of a single phase DAB and reduce the reactive circulating currents. However, piecewise linear time analysis requires complicated multi-modal steady-state analysis when adaptive modulation concepts are used with a single phase DAB. Thus, the design process has to inevitably deal with a complex sequence of operating modes. This leads to a fractional modeling process which does not achieve simple and comprehensive guidance on how the DAB is expected to perform across the entire operating range. Beyond that, practical switching effects such as modulator dead-time or device parasitic capacitances have to be evaluated separately for each operating mode condition.

Finally it is also observed that the literature has primarily focused on the analysis of the AC link active bridge circuits and passive power devices, with the DC bus and its filter elements only mentioned in relation to control aspects. As a consequence, the consideration of the DC bus waveforms and its
filter impedances remains a rather untouched topic in the literature, although, unlike other non-isolated DC-DC or DC-AC converters [105] [106], the Phase Shifted Square Wave (PSSW) modulation strategy injects substantial harmonic distortion into the DC bus at integer multiples of the switching frequency. This distortion interacts with the parasitic filter impedances to potentially cause a resonance hazard and subsequent operation failure. However until now, no publication has reported the DC side filter design difficulties which become more and more severe as operating frequencies further increase and the converter behavior becomes less ideal.

The literature review has also outlined several examples where the DAB converter model was extended to include single impedance or switch non-idealities, advanced modulation strategies and passive device models, and thus satisfy any application context. However it still lacks a complete and powerful analysis framework which can combine all these effects. This new modeling technique should be able to broadly accommodate all ZVS boundary conditions and power transfer modes, and handle adaptive DAB modulation concepts and complex AC coupling impedances, together with other practical switching effects such as phase leg dead-time delay and parasitic device capacitance. In a next step, the method should then be able to identify distinct design and operation guidelines to achieve best possible DAB performance. The three major research questions (RQ) for this thesis are hence expressed as follows:

- **RQ 1)** Can frequency domain analysis of a DAB be used to determine more general and precise ZVS boundary expressions for single and three-phase DABs, taking into account complex impedance models, advanced multi-level modulation concepts and practical converter non-idealities?

- **RQ 2)** Can the proposed analysis strategy provide immediate design and operation guidance on how to achieve continuous low-loss ZVS operation of a practical DAB converter despite limiting factors such as the non-ideal switching behavior?

- **RQ 3)** Can the established framework also include DC bus current harmonics and parasitic second order DC bus impedances into the design process, and show how modulation influences the DC bus frequency components?
3 Determination of Zero Voltage Switching (ZVS) Regions For Single Phase DAB

The only way to further enhance the power density and cost-effectiveness of any power-electronic converter is to increase its operating frequency, unless the material specifications of passive power devices and/or the thermal cooling capability drastically evolve. Hence, for a DAB, precisely identifying the ZVS boundary conditions for any design and operating context is key to minimising the switching energies that need to be dissipated. This requires the practicalities of the AC link coupling network (in particular the transformer) and the non-ideal switching process to become more relevant in the entire design process. Hence, these effects have to be included into the analysis to accurately determine the available ZVS operating range. However, a DAB is conventionally designed using time domain analysis which typically presumes an idealized single parameter AC link inductance and switch transition to evaluate the ZVS condition of a DAB. Recognising that this analysis technique only approximates the more complex model of a practical DAB high-frequency (HF) transformer, it does not allow to design for more complex AC link coupling impedances. More recent work has begun to consider harmonic analysis strategies to overcome these limitations. However, to date these approaches have only been proposed using a fundamental component approximation [107], or have not developed an analytical closed form solution for the ZVS range of the DAB [108].

This chapter now presents a new theoretical approach using harmonic analysis to analytically determine the ZVS boundary conditions of a single DAB converter across the entire range of operating conditions. This can then be used to accurately determine the ZVS boundaries for any particular DAB design and operating context, by identifying the precise conditions of the PSSW (Phase Shifted Square Wave) phase shift angle, the PSSW duty cycles, the AC coupling impedance and the bridge DC bus voltage levels.

The new approach separates the two bridge voltage switching patterns into their harmonic equivalent forms, and then calculates the inter-bridge circulating current(s) as a set of harmonic components flowing through a generic two-port admittance network. Each harmonic is expressed as an individual function of the bridge DC bus voltages and the PSSW phase shift and duty cycle angles. The summation of these current harmonics is then evaluated to determine the polarity of each bridge current as their switches

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1 Material in this chapter was first published in:
change state, to identify whether ZVS has occurred for the conditions considered. This analysis strategy readily allows more complex bridge coupling networks, practical impedance non-idealities [109] and non-ideal switching effects [33] [110] such as dead-time and parasitic device capacitance, and advanced modulation strategies to be included. Next, reduced analytical closed form solutions are presented for single and three-phase DAB operation with a single ideal coupling inductance, matched against conventional time domain solutions to confirm the validity of the approach. Finally, more advanced results using numerical integration are presented with predicted ZVS conditions confirmed by experimental investigations.

3.1 Fundamentals

The general structure of a single phase DAB is shown in Fig. 3.1(a), where the primary and secondary side converters are connected via a general two-port admittance \( Y \). Fig. 3.1(b) shows an exemplar DAB coupling network, consisting of a HF two-winding transformer with primary and secondary series resistances and leakage inductances, and a central magnetising inductance. For the DAB topology, the phase legs of each bridge are switched with 50% duty cycle square waves. For a single phase DAB these are typically displaced exactly 180° out of phase, to create an AC square wave output (2-level modulation). The two bridge outputs are then displaced by a phase shift angle \( \delta \) to provide a single control degree of freedom. For an ideal series AC link coupling inductance, active power is transferred from the primary to the secondary bridge if \( \delta > 0 \) and vice versa. This strategy is known as Phase Shifted Square Wave (PSSW) modulation. DAB operational flexibility using 2-level PSSW modulation is relatively constrained because the volt-second output of each bridge is always proportional to its DC bus voltage.

In contrast, adaptive 3-level DAB modulation introduces two additional degrees of freedom by no longer constraining the phase leg switching of each bridge to be displaced by \( \pi \) (radians). This produces reduced duty cycle quasi-square wave outputs for each bridge, offering the benefits of a reduced magnitude reactive power circulating current because of the variable bridge volt-second output, and extended ZVS regions of operation across a wider range of DC bus voltage variation for each bridge. Typical 3-level switching patterns for a single phase DAB are shown in Fig. 3.1(c), where \( \delta \) is the displacement angle between the centre points of the output pulses of the two bridges, and \( \alpha \) and \( \beta \) are the primary and secondary bridge duty cycle angles, respectively.

For either (single phase or three-phase) DAB topology, ZVS will occur if the output current of a bridge is flowing through the active switch of its phase leg as the phase leg changes state, since the current will then naturally commute to the opposing switch anti-parallel diode. With respect to the definitions in Fig. 3.1(c), the outgoing phase leg current has to be (sufficiently) negative for a positive phase leg transition (from low-side to high-side switch) and positive for a negative phase leg transition (from high-side to low-side switch). Note that HB1 is hard-switched for the single phase DAB in Fig.
CHAPTER 3. DETERMINATION OF ZVS REGIONS (SINGLE PHASE DAB)

(a) Topology

(b) AC coupling impedance

(c) Phase leg switched voltages and bridge output currents

Figure 3.1: Single Phase DAB

1(c), since its current is positive for the positive phase leg transition. Note also that the currents through the primary and secondary transformer coils are not exactly matched in these figures, since a finite magnetising impedance has been deliberately included into the coupling network. Operating
the phase legs under ZVS facilitates the use of higher switching frequencies and state-of-the-art silicon-based Power MOSFET technologies such as super-junction FETs, or up-coming wide bandgap devices, in particular SiC and GaN, since a ZVS transition significantly reduces the switching losses in most cases. Note also that since ZCS (Zero Current Switching) occurs just at the boundary of ZVS, it can be classified as a subcategory of ZVS for this topology and does not need to be considered separately.

Fig. 3.2 (a) shows the switched voltages and device currents for the first leg of the primary bridge, i.e. HB1 (switches $S_{p,1}$ and $S_{p,2}$), for a hard switching (current flowing through $S_{p,2}$ diode before switching) negative-to-positive phase leg voltage transition. For a hard switching transition outside ZVS, the load current commutates from the outgoing anti-parallel diode of $S_{p,2}$ to the active device of $S_{p,1}$, and the drain-source (and any externally paralleled) capacitance must be rapidly discharged during the active device turn-ON. The reverse recovery charge of the outgoing diode also causes high switching losses and increased thermal stress of the switch device. Fig. 3.2 (c) then shows the switched voltages and device currents for a ZVS soft switching (current flowing through $S_{p,2}$ active device before switching) negative-to-positive phase leg voltage transition. For a ZVS transition, the phase leg voltage naturally rises as $S_{p,2}$ is turned OFF as the device capacitance is charged by the (negative) load current $i_p$. The upper anti-parallel diode of $S_{p,1}$ then turns ON (almost) losslessly, clamping at the positive DC rail voltage. Figs. 3.2 (b) and (d) then illustrate the respective current path sequences for a hard and soft switching transition.

The ZVS regions for each bridge vary as a function of the primary and secondary bridge DC bus voltages $V_{p,DC}$ and $V_{s,DC}$, the bridges’ output duty cycle angles $\alpha$ and $\beta$, the phase shift angle $\delta$ between the bridges, and the AC coupling impedance network. Precisely determining these boundaries as operating conditions vary is essential for effective design and high efficiency operation of a DAB converter. Given that a square wave can be readily expressed as a direct summation of odd harmonics through a Fourier series expansion, it immediately follows that the phase leg output voltages of a single phase 3-level modulated DAB can be expressed in harmonic form as

\[
\begin{align*}
v_{HB1}(t) &= \frac{4V_{p,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{[2n-1]} \sin \{([2n-1]w_{swt} + \alpha/2) \} \\
v_{HB2}(t) &= \frac{4V_{p,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{[2n-1]} \sin \{([2n-1]w_{swt} - \alpha/2) \} \\
v_{HB3}(t) &= \frac{4V_{s,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{[2n-1]} \sin \{([2n-1]w_{swt} + \beta/2 - \delta) \} \\
v_{HB4}(t) &= \frac{4V_{s,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{[2n-1]} \sin \{([2n-1]w_{swt} - \beta/2 - \delta) \}
\end{align*}
\]  

(3.1)

where $N \to \infty$ and the voltages $v_{HBi}(t)$ define the $i^{th}$ phase leg’s output voltage referred to its corresponding DC bus voltage midpoint, $i \in \{1, 2, 3, 4\}$. The secondary bridge DC bus voltage can also be expressed as a proportion of the primary bridge DC bus voltage as $V_{s,DC} = dV_{p,DC}$ (note that without loss of generality, the turns ratio $N_s/N_p$ equals unity in the following analysis).
CHAPTER 3. DETERMINATION OF ZVS REGIONS (SINGLE PHASE DAB)

(a) Hard switching event: characteristic waveforms

(b) Hard switching: diode-to-switch commutation sequence

(c) ZVS event: characteristic waveforms

(d) ZVS: switch-to-diode commutation sequence

Figure 3.2: Hard vs. soft switched phase leg transition (HB1)
AC coupling network can now be expressed using two port circuit analysis as follows:

\[
\begin{bmatrix}
i_p(t) \\
i_s(t)
\end{bmatrix} = \begin{bmatrix}
y_{p,p}(t) & y_{p,s}(t) \\
y_{s,p}(t) & y_{s,s}(t)
\end{bmatrix} \begin{bmatrix}
v_p(t) \\
v_s(t)
\end{bmatrix}
\]  

(3.2)

where \(y_{p,s}(t)\) is a self or mutual (as appropriate) admittance defined in terms of the coupling network resistances (gain terms), inductances (integral terms) and capacitances (derivative terms). The individual matrix elements can be defined according to (3.12) for the monotonic transformer equivalent circuit in Fig. 3.1(b). The primary and secondary bridge output voltages \(v_p(t)\) and \(v_s(t)\) are given by

\[
v_p(t) = v_{HB1}(t) - v_{HB2}(t)
\]

\[
v_s(t) = v_{HB3}(t) - v_{HB4}(t)
\]

(3.3)

For each of the harmonic frequencies defined in (3.1), the time varying relationships between the bridge voltages and currents (3.2) can be expressed using AC phasor theory as follows:

\[
\begin{bmatrix}
i_p^m(\theta_p^m) \\
i_s^m(\theta_p^m)
\end{bmatrix} = \frac{4V_{p,DC}}{\pi m} \begin{bmatrix}
y_{p,p}^m & y_{p,s}^m \\
y_{s,p}^m & y_{s,s}^m
\end{bmatrix} \begin{bmatrix}
1 \{m|\gamma/2\} - 1 \{m|\gamma/2 - \delta\} \\
d \{m|\gamma/2 - \delta\} - d \{m|\gamma/2 - \delta - \delta\}
\end{bmatrix}
\]

(3.4)

where the superscript \(m = [2n - 1]\) defines the harmonic frequency \(mw_{sw}\) and the voltages, currents and admittance matrix elements are expressed in complex angular form. The overall bridge currents can then be expressed in time domain by transforming this phasor solution back into a sinusoidal steady-state time varying form for each harmonic frequency, and summing these solutions across all frequencies to give

\[
i_p(w_{sw}t) = \sum_{n=1}^{\infty} i_{p}^m(w_{sw}t) = \frac{4V_{p,DC}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \times
\]

\[
\begin{cases}
y_{p,p}^m \{\sin (m|w_{sw}t + \alpha/2| + \gamma_{p,p}^m) - \sin (m|w_{sw}t - \alpha/2| + \gamma_{p,p}^m)\} \\
+ dY_{p,p}^m \{\sin (m|w_{sw}t + \beta/2 - \delta| + \gamma_{p,p}^m) - \sin (m|w_{sw}t - \beta/2 - \delta| + \gamma_{p,p}^m)\}
\end{cases}
\]

(3.5a)

\[
i_s(w_{sw}t) = \sum_{n=1}^{\infty} i_{s}^m(w_{sw}t) = \frac{4V_{p,DC}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \times
\]

\[
\begin{cases}
y_{s,p}^m \{\sin (m|w_{sw}t + \alpha/2| + \gamma_{s,p}^m) - \sin (m|w_{sw}t - \alpha/2| + \gamma_{s,p}^m)\} \\
+ dY_{s,p}^m \{\sin (m|w_{sw}t + \beta/2 - \delta| + \gamma_{s,p}^m) - \sin (m|w_{sw}t - \beta/2 - \delta| + \gamma_{s,p}^m)\}
\end{cases}
\]

(3.5b)

The ZVS boundary for each bridge phase leg positive voltage transition (negative transition is sym-
CHAPTER 3. DETERMINATION OF ZVS REGIONS (SINGLE PHASE DAB)

metrical and so does not need to be considered) can then be mathematically expressed as follows:

\[ i_p(w_{sw} t = \alpha/2) \leq 0 \quad \text{(HB1)} \]
\[ i_p(w_{sw} t = \alpha/2) \geq 0 \quad \text{(HB2)} \]
\[ i_s(w_{sw} t = -\beta/2 + \delta) \leq 0 \quad \text{(HB3)} \]
\[ i_s(w_{sw} t = \beta/2 + \delta) \geq 0 \quad \text{(HB4)} \]

Equation (3.7) identifies the conditions under which ZVS occurs for each phase leg, as an exact analytical relationship between the PSSW modulation angles \( \alpha \), \( \beta \) and \( \delta \), and the DC bus voltage ratio \( d \) of the two bridges, for any coupling admittance network between the bridges.

When \( \alpha = \beta = \pi \), the AC phasor relationship between the bridge switched output voltages and the outgoing phase leg currents flowing into the coupling network reduces to

\[
\begin{bmatrix}
I_{m,p}^m \angle \theta_{p,m}^m \\
I_{m,s}^m \angle \theta_{s,m}^m 
\end{bmatrix} = \frac{8V_{p,DC}}{\pi m} \times \begin{bmatrix}
Y_{p,p,m}^m \angle \gamma_{p,p,m}^m \\
Y_{s,s,m}^m \angle \gamma_{s,s,m}^m
\end{bmatrix} \begin{bmatrix}
1 \angle m\frac{\pi}{2} \\
1 \angle m\left[\frac{\pi}{2} - \delta\right]
\end{bmatrix}
\]

The ZVS region is then defined by an (upper) primary bridge boundary, (3.9a), and a (lower) secondary bridge boundary, (3.9b), as an exact relationship between the converter DC-DC voltage ratio
2.2 LEVEL VS. 3-LEVEL MODULATION

As identified earlier, the analytical determination of ZVS in the time domain for 3-level modulation is quite challenging, with up to 12 modes of operation required to determine ZVS limits at any particular operating condition [39]. In contrast, the harmonic analysis approach presented here results in a single coherent solution for the ZVS boundary conditions across the entire converter operating range. Fig. 3.3 demonstrates this capability, by showing the effect of changes of the 3-level modulation angles on the ZVS boundaries as the voltage conversion ratio \( d \) and the PSSW phase shift angle \( \delta \) vary, for an ideal series inductance AC link network.

From this figure, it can be seen how the linked ZVS boundary curves established for each bridge under 2-level modulation (Fig. 3.3(a)) change as either the secondary (Fig. 3.3(b)) or primary (Fig.
3.3(c)) bridge is 3-level modulated. In particular, the ZVS boundary curves for each of the phase legs of the 3-level modulated bridge diverge with respect to the phase shift angle $\delta$, and also shift upwards or downwards away from the nominal DC bus voltage ratio of $d = 1$ in proportion to the $\alpha/\beta$ ratio. As shown in Figs 3.3(b) and 3.3(c), these changes create an additional ZVS region, centered about $\delta = 0$, which is connected to the higher power ZVS regions through singular “cusp” points which occur at the off-nominal DC bus voltage ratio defined by the $\alpha/\beta$ ratio. Consequently this ratio must always be adjusted to match the physical DC bus voltage ratio when transitioning from the central lower power ZVS region ($|\delta| \leq |\alpha - \beta|$) to the higher power ZVS regions ($|\delta| \geq \pi - |\alpha + \beta|$), to ensure continuous ZVS operation through these cusp points. This process will be further discussed in Chapter 5. Also note that within this higher power region the ZVS boundary of the 2-level modulated bridge remains according to (3.11) irrespective of the 3-level PSSW duty cycle of the other bridge. However, as can be seen from the figures, 3-level modulation results in a segmentation of the ZVS boundary curves due to the change in switching sequence between the primary and secondary bridge phase legs.

In addition, as shown in Fig. 3.3(d), the effect of 3-level modulating both bridges by the same amount (i.e. $\alpha/\beta$ remains equal to 1) is to create a long singular ZVS connection boundary between the two higher power ZVS regions, which precludes ZVS operation for lower values of $|\delta|$ if the DC bus
3.3 ZVS Analysis for Non-Ideal AC Coupling Impedances

To illustrate the capability of the harmonic analysis strategy, the ZVS boundary conditions are evaluated for a single phase DAB converter with different AC coupling impedances and PSSW modulation parameters. The complex admittance matrix elements of \([Y]\) for a primary-side referred inductive-ohmic transformer model (Fig. 3.1) become
\[ Y_{m,n}^{p,p} = \frac{I_m}{V_n^{p,p}}|Y_{p,s}^{n}=0 = Y_{m,s}^{p,s} \cdot \frac{j m w_{sw} (L_{m}^{p,p} + L_{m,s}^{n}) + R_{m,s}^{n}}{-j m w_{sw} L_{m}^{p,p}} \]

\[ Y_{m,n}^{p,s} = \frac{I_m}{V_n^{p,s}}|Y_{p,s}^{n}=0 = -j m w_{sw} L_{m}^{p,s} \]

\[ Y_{m,n}^{s,p} = \frac{I_m}{V_n^{s,p}}|Y_{p,s}^{n}=0 = Y_{m,s}^{p,s} \cdot \frac{j m w_{sw} (L_{m}^{s,p} + L_{m,s}^{n}) + R_{m,s}^{n}}{-j m w_{sw} L_{m}^{p,p}} \]

Remark: \( L_{m,s}^{p,p} = L_{m,s}^{n} + L_{m,s}^{p,s} \quad R_{m,s}^{n} = R_{m,s}^{p} + R_{m,s}^{n} \) (3.12)

For the experimental system (described in more detail in Chapter 9), the AC coupling impedance was connected directly between the IGBT switched primary and secondary bridges. The bridges were operated in open loop mode, switching at 20 kHz (limited by the available experimental bridge), with the PSSW displacement angles adjusted manually from the controlling computer. The DC buses were created by standard DC power supplies, with paralleled load resistors to allow energy to be absorbed at the receiving bridge. The asymmetric forward voltage drop across the IGBT devices and the anti-parallel diodes (voltage inherently reverses with current polarity) was used to precisely identify switching transition types from the bridge output voltage patterns, i.e. from diode to switch (hard switching), from diode to diode (ZVS boundary), from switch to diode (ZVS soft switching). The operating points presented here have been selected so that dead-time has no effect on the ZVS regions as will be identified in Section 3.4.

### 3.3.1 Significant Resistance in the AC Link

The capability of the proposed harmonic analysis approach is first demonstrated by exploring the changes in the ZVS regions when a non-ideal coupling inductance with a significant series resistance (\( RL \)) is used, compared to an (almost) purely inductive load (\( L \)), for 2-level PSSW operation (\( \alpha = \beta = \pi \)). Note that the resistance of the transformer is determined in practice by various influences such as the conducting material, the winding technique, the geometry of the core and the winding, and the applied switching frequency. If the coupling network is simplified for an \( RL \) coupled inductor impedance according to Fig. 3.5 (i.e. no vertical magnetising current path), the matrix elements for \([Y]\) reduce as follows:

\[ Y_{m,n}^{p,p} = Y_{m,n}^{p,s} = Y_{m,n}^{s,p} = Y_{m,n}^{s,s} = \frac{1}{R + j m w_{sw} L} \] (3.13)

![Figure 3.5: Simplified RL impedance network](image-url)
For this example, the DAB is operated with a single inductor of 0.53 mH (experimental details described in Chapter 9) and a substantial series resistance of 14 Ω, to clearly show the resistance effect. Fig. 3.6(a) and 3.6(b) show how the ZVS boundaries skew vertically when the resistance is in circuit, depending on the sign of $\delta$. Hence the impact of series resistance is a reduction of the ZVS voltage range capability of the converter for bi-directional power flow (it is commented that there is a complex relationship between the active power transfer and $\delta$ when resistive elements are included, as will be further discussed in Chapter 7).

This predicted result has been confirmed using a time-domain based circuit simulation with results shown in Fig 3.6(c) and with the experimental waveform shown in Fig. 3.6(d). It can be seen that when $d$ equals 0.58, ZVS is not achieved for $\delta = \frac{\pi}{6}$ with an ideal coupling inductance, as shown by the hard switching transition in the secondary bridge voltage waveform, while the introduction of series resistance moves the operating condition (test point OP$_1$) back into ZVS. Note however that this improvement in ZVS boundary for a positive sign of $\delta$ impacts adversely on the ZVS boundary regions for the reverse direction.

Fig. 3.7(a) shows how the ZVS boundaries for this system vary for the two alternative impedances as a function of the DC bus voltage ratio $d$ and control angle $\delta$, for adaptive 3-level PSSW modulation with the bridge duty cycles of $\alpha = \frac{\pi}{2}$ and $\beta = \frac{2\pi}{3}$. As already observed for 2-level PSSW modulation, the AC link resistance moves the boundaries vertically depending on the sign of $\delta$. The operating conditions of
3.3.2 Transformers with Variable Winding Coupling

The influence of transformer winding coupling was explored by considering a transformer with a variable coupling coefficient. Special U-core ferrite test transformers with a unity turns ratio and adjustable winding coupling were made. Table 3.1 lists the leakage inductances and magnetising inductances for three alternative physical transformer configurations that were measured using the techniques described in [112] (design specifications in Chapter 9). The resultant ZVS boundaries for T1 and T3 in Fig. 3.8 show that a reduced winding coupling (leakage inductances remain essentially constant while the magnetising inductance reduces) increases the separation between the primary bridge phase leg ZVS boundaries (HB1 and HB2) and the secondary bridge ZVS boundaries (HB3 and HB4). This significantly increases the available ZVS region and enables overall practical soft switching (incl. second order effects) for any DAB steady-state system condition of power and input vs. output voltage.
3.3. ZVS ANALYSIS FOR NON-IDEAL AC COUPLING IMPEDANCES

Figure 3.8: ZVS boundaries for T1 and T3 over $\delta$ ($\alpha = \frac{2\pi}{3}$, $\beta = \frac{3\pi}{4}$)

Figure 3.9: Experimental validation of coupling impact: $\delta = \frac{\pi}{6}$ and $d = 0.7$

Note that in a physical sense, such a reduction in the winding coupling can be caused by factors such as a less compact winding technique (stray flux increases) or an extended core gap (magnetising inductance decreases) recognising that a minimum airgap is essential to manage dc flux generation caused by the switching process of both transient and steady-state operation [113] [114] even if a DC flux compensation technique is applied to such ZVS soft switched type converters suffering from a volt-second bridge modulation mismatch [89].

Operating point OP₃ in Fig. 3.8 predicts that the HB4 devices will be hard switching for T1 (under the conditions listed), but will be soft switching for the reduced coupling factor transformer T3. The experimental waveforms presented in Fig. 3.9 confirm this result, with the secondary current positive at the negative HB4 transition in Fig. 3.9(a) with T1, and clearly negative at the same transition in Fig. 3.9(b) with T3. Note that the secondary current waveform shown in Fig. 3.9 is the inverse of the reference polarity secondary current.

Similarly, the distribution of leakage flux between the primary and secondary coils is influenced by factors such as the compactness of the winding material (e.g. foil vs. round wire) and by the location

<table>
<thead>
<tr>
<th>Imp.</th>
<th>$L_m(\mu H)$</th>
<th>$L_{\sigma,p}(\mu H)$</th>
<th>$L_{\sigma,s}(\mu H)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>312.6</td>
<td>49.6</td>
<td>39.9</td>
</tr>
<tr>
<td>T2</td>
<td>302.3</td>
<td>41.7</td>
<td>52.9</td>
</tr>
<tr>
<td>T3</td>
<td>101.5</td>
<td>46.1</td>
<td>34.3</td>
</tr>
<tr>
<td>T4</td>
<td>85.7</td>
<td>35.2</td>
<td>51.7</td>
</tr>
</tbody>
</table>

Table 3.1: Measured transformer impedances (T1-T4)
Figure 3.10: ZVS boundaries for T3 and T4 over δ (α = \(\frac{2\pi}{3}\), β = \(\frac{3\pi}{4}\))

Figure 3.11: Experimental validation of coupling impact: δ = \(-\frac{\pi}{3}\) and d = 1.3

of the individual coils in relation to the high permeability magnetic path (i.e. the core). In Figs. 3.10 and 3.11 a similar coupling factor is selected, however the ratio between primary and secondary coil’s leakage inductances inverses, which shifts up/down the ZVS boundaries in favor to the converter bridge that is connected to the lower leakage transformer coil. This results in an asymmetric ZVS region with respect to the unity DC-DC voltage ratio (i.e. d =1). Thus, the ratio between the individual coil stray inductances immediately correlates with the selected (physical) turns ratio. For operating condition OP4, the experimental results shown in Fig. 3.11 again confirm the theoretical expectations of Fig. 3.10, which are that T3 operates very close to the ZVS boundary while T4 is comfortably in the ZVS region.

### 3.4 Impact of Practical Switching Issues on ZVS Boundaries

The major practical switching issues that significantly impact ZVS operation of a DAB converter are dead-time and device output capacitance. Dead-time is the delay between turn-OFF of the outgoing active switch of a phase leg, and turn-ON of its matching incoming switch, which is required to avoid the shoot-through current pulse through the phase leg that typically occurs if the phase leg devices are simultaneously switched, because of unequal switching delays. Device capacitance influences the rise/fall slew rate of the phase leg switched voltage when the phase leg changes state, with the overall rise/fall time for a switching event being a complex interaction between device capacitance, DC bus voltage magnitude and phase leg current.

Both effects can significantly change the real ZVS boundaries for a DAB away from their theoretical
determination, particularly at high switching frequencies using wide band-gap devices where dead-time can be a large proportion of the fundamental period. Hence their influence needs to be accommodated by the analysis procedure if ZVS boundaries are to be accurately predicted for a physical DAB. While this is very difficult to achieve using time domain analysis, the harmonic analysis strategy presented here is readily adapted to include these practical influences, as will now be explained.

3.4.1 Dead-Time Influence on ZVS Transition

Ideally, and as assumed in (3.6), a ZVS transition occurs if the phase leg current is the correct polarity to make the phase leg voltage immediately change state as its outgoing device turns OFF, i.e. a negative phase leg current will cause an immediate negative-to-positive phase leg voltage transition as the low-side device is turned OFF (this transition is of course clamped at \(+V_{DC}\) by the high-side anti-parallel diode becoming forward biased). In practice however, the phase leg current magnitude has to be sufficiently larger than zero to avoid it crossing zero during the dead-time delay period \(\rho DT\) and causing an erroneous hard switching event [115], as shown in Fig. 3.12. In Fig. 3.12(a), it can be seen how the phase leg current has become positive during the dead-time period after the low-side device has been turned OFF and before the high-side device has been turned ON. This polarity change causes the phase leg voltage transition to reverse back to \(-V_{DC}\), and partial hard switching then occurs when the high-side device is eventually turned ON. In contrast, Fig. 3.12(b) shows the smooth successful ZVS transition that occurs when the phase leg current at the moment of low-side device turn OFF, has sufficient magnitude to remain negative during the entire dead-time period \(t_{DT}\). The unsuccessful ZVS event shown in Fig. 3.12(a) is quite undesirable in terms of device thermal stress and bridge controllability, both because of the multiple switching transitions, and the diode reverse recovery loss caused by the hard switching transition. In addition, dead-time causes PSSW modulation errors if a phase leg is operated outside ZVS, which need to be compensated by the controller as discussed in [96] [98] [116].

The harmonic ZVS analysis approach can be readily adapted to include the effect of dead-time by
simply changing the angular time at which ZVS is required to occur, from (3.6) to

\[ \max_r \{ i_p(w_{sw}t = -\alpha/2 + r \cdot \rho_{DT_p}) \} \leq 0 \quad (HB1) \] (3.14a)

\[ \min_r \{ i_p(w_{sw}t = \alpha/2 + r \cdot \rho_{DT_p}) \} \geq 0 \quad (HB2) \] (3.14b)

\[ \max_r \{ i_s(w_{sw}t = -\beta/2 + \delta + r \cdot \rho_{DT_s}) \} \leq 0 \quad (HB3) \] (3.14c)

\[ \min_r \{ i_s(w_{sw}t = \beta/2 + \delta + r \cdot \rho_{DT_s}) \} \geq 0 \quad (HB4) \] (3.14d)

where \( \rho_{DT_p} \) and \( \rho_{DT_s} \) are the respective dead-time angles used for the primary bridge phase legs (HB1 and HB2) and the secondary bridge phase legs (HB3 and HB4), and \( r = [0 : 1] \) determines whether or not dead-time is taken into account. Analytically, the condition from (3.14) can be conveniently accommodated back into (3.6) substituting the resulting summation within the sine argument of (3.5), i.e. \( mr \cdot \rho_{DT_x} + \gamma_{m,x} \), by a modified admittance matrix element phase angle \( \gamma_{m,x} \), to give

\[ \gamma_{m,r,x} = \gamma_{m,x} + mr \cdot \rho_{DT_x} \quad x \in \{ p, s \} \] (3.15)

into (3.5), which allows the same 3-level modulation parameters \( \alpha \) and \( \beta \), phase shift angle \( \delta \) and voltage DC-DC conversion ratio \( d \), to be used. The ZVS boundary condition of (3.7) then becomes (HB1 only shown)

\[ d_{DT}^{\text{HB1}}|_{\text{ZVS}} = \min_r \left\{ \sum_{n=1}^{\infty} \frac{Y_{m,n}^{m,p}}{m} \left\{ \sin \left( \gamma_{n,p} \right) \cos (m\alpha) - \cos \left( \gamma_{n,p} \right) \sin (m\alpha) - \sin \left( \gamma_{n,p} \right) \right\} \right\} \]

\[ \quad \left\{ \frac{2}{m} \sum_{n=1}^{\infty} \frac{Y_{m,n}^{m,s}}{m} \left\{ \cos \left( \gamma_{n,s} \right) \cos (m\delta + \frac{\pi}{4}) + \sin \left( \gamma_{n,s} \right) \sin (m\delta + \frac{\pi}{4}) \right\} \right\} \] (3.16)

Fig. 3.13 shows how dead-time affects the ZVS regions for both 2-level and (primary bridge) 3-level DAB operation, by skewing the primary bridge ZVS boundaries to the right when \( d > 1 \) and the
secondary bridge ZVS boundaries to the left when \( d < 1 \). The consequence is a reduction in the available ZVS regions for particular operating conditions, which has to be taken into account when analysing the ZVS operating range of a DAB. Note also that the worst case of the conditions of “without dead-time” \( (r = 0) \) and “with dead-time” \( (r = 1) \) must always be used to determine the ZVS boundaries, since the phase leg current must have the correct (and same) polarity during the entire dead-time period to successfully complete a ZVS transition.

### 3.4.2 Significant Device Output Capacitance

For semiconductor devices with a relatively large output capacitance, or if an external snubber capacitor is added to “soften” the phase leg voltage slew rate, a minimum phase leg current magnitude is required during the dead-time period to ensure a complete ZVS phase leg voltage transition to the other DC bus before the incoming device is turned ON. If a phase leg is operated very close to its ZVS boundary as determined by (3.14), the consequential small current magnitude at the start of the switching event may cause the phase leg voltage to slew slowly during the dead-time period and cause an incomplete phase leg voltage transition and thus a partial hard switching outcome. This is shown in Fig. 3.14(a) for HB1 (same for HB2) under 2-level modulation and power flow from primary to secondary \( (\delta > 0) \), and in Fig. 3.14(c) for power flow from secondary to primary \( (\delta < 0) \). This influence of device capacitance can be readily integrated into the harmonic analysis process by changing the ZVS limit conditions from (3.14) to

\[
\begin{align*}
\max_r \{i_p(w_{sw}t = -\alpha/2 + r \cdot p \cdot \rho t_p)\} &\leq -\Delta i_p \quad \text{(HB1)} \\
\min_r \{i_p(w_{sw}t = \alpha/2 + r \cdot p \cdot \rho t_p)\} &\geq \Delta i_p \quad \text{(HB2)} \\
\max_r \{i_s(w_{sw}t = -\beta/2 + \delta + r \cdot p \cdot \rho t_s)\} &\leq -\Delta i_s \quad \text{(HB3)} \\
\min_r \{i_s(w_{sw}t = \beta/2 + \delta + r \cdot p \cdot \rho t_s)\} &\geq \Delta i_s \quad \text{(HB4)}
\end{align*}
\]

where \( \Delta i_p \) and \( \Delta i_s \) are the minimum (absolute) phase leg current magnitudes that must be maintained during a dead-time period to inject sufficient charge into the phase leg device capacitances to reliably achieve a ZVS bus-to-bus voltage transition.

For example, the requirement for the HB1 phase leg transition as shown in Fig. 3.14(b) is given by \( Q_p = \int_0^{2V_{DC}} C_{HB1}(v_{HB1}^*)dv_{HB1}^* \leq \Delta i_p \cdot t_{DT_p} \) (note that this is a conservative estimate since the charge delivered by the actual time varying \( i_p(t) \) during the dead-time period will be greater than \( \Delta i_p \cdot t_{DT_p} \)). The total phase leg capacitance \( C_{HB1} \) has to be carefully determined, in particular for a non-linear (voltage-variant) output capacitance [117]. Fig. 3.14(d) then illustrates the equivalent requirement under negative power transfer conditions \( (\delta < 0) \). Note also that a margin usually needs to be added to \( \Delta i_p \) and \( \Delta i_s \) to account for the change in \( Q_p \) required as a function of the DC bus voltage magnitude, and the fraction of \( i_p(t) \) flowing through the out-going device that does not contribute to device capacitor charge (e.g. IGBT tail current).

These two separate issues of maintaining the correct phase leg current polarity throughout the entire
dead-time period to avoid a double voltage transition, and ensuring a minimum current magnitude to guarantee that the device capacitances charge up to the opposite DC bus during this period, can now be combined together into one mathematical expression. The effective practical ZVS operating range then becomes

\[
d_{\text{ZVS}}^{\text{HB1}} \leq \min_r \left\{ \sum_{n=1}^{\infty} \frac{Y_n}{m} \left\{ \sin \left( \gamma_{p,r} \right) \cos \left( \theta_n \right) - \cos \left( \gamma_{p,r} \right) \sin \left( \theta_n \right) \right\} - \frac{\pi \Delta_{\text{p},r}}{4V_{\text{p,DC}}} \right\} \tag{3.18a}
\]

\[
d_{\text{ZVS}}^{\text{HB2}} \leq \min_r \left\{ \sum_{n=1}^{\infty} \frac{Y_n}{m} \left\{ \cos \left( \gamma_{p,r} \right) \cos \left( \theta_n \right) + \sin \left( \gamma_{p,r} \right) \sin \left( \theta_n \right) \right\} + \frac{\pi \Delta_{\text{p},r}}{4V_{\text{p,DC}}} \right\} \tag{3.18b}
\]

\[
d_{\text{ZVS}}^{\text{HB3}} \geq \max_r \left\{ \sum_{n=1}^{\infty} \frac{Y_n}{m} \left\{ \sin \left( \gamma_{p,r} \right) \cos \left( \theta_n \right) - \cos \left( \gamma_{p,r} \right) \sin \left( \theta_n \right) \right\} \right\} \tag{3.18c}
\]

\[
d_{\text{ZVS}}^{\text{HB4}} \geq \max_r \left\{ \sum_{n=1}^{\infty} \frac{Y_n}{m} \left\{ \cos \left( \gamma_{p,r} \right) \sin \left( \theta_n \right) + \sin \left( \gamma_{p,r} \right) \cos \left( \theta_n \right) \right\} + \frac{\pi \Delta_{\text{p},r}}{4V_{\text{p,DC}}} \right\} \tag{3.18d}
\]

Figure 3.14: Phase leg voltage transition of HB1 for different switched current magnitudes (sketch)
3.5 Summary

This chapter presented a new theoretical approach to analytically determine the ZVS boundary conditions of a single phase DAB, by harmonic decomposition of the bridge output voltage patterns and the usage of a generic two-port AC link network. This approach has then been applied to accurately investigate the ZVS boundaries for any particular DAB design and operating context, by identifying the precise relationship between the modulation angles and the bridge DC bus voltage levels. Numerical integration is used to illustrate how complex bridge coupling networks, non-ideal switching effects and 3-level PSSW bridge modulation influence the ZVS boundary conditions. Appendix A shows how the presented theory can be applied in a reverse-type manner to precisely estimate the AC coupling impedance parameters during converter operation.
This chapter now determines the ZVS boundary conditions of a three-phase DAB under all operating conditions using harmonic analysis. Similarly to the single phase DAB approach in Chapter 3, the analysis of the balanced three-phase DAB system begins by expressing the two-level phase leg switching waveforms for each three-phase bridge as a summation of harmonics that vary according to the primary and secondary bridge DC bus voltages and the Phase Shifted Square Wave (PSSW) displacement angle between the bridges.

However, practical three-phase transformers are commonly designed with three or five core legs. Typically, the geometry causes unbalanced leakage impedances, since the mutual and leakage flux relationship generated by one pair of phase coils differs compared to the others [93]. By extending the harmonic analysis strategy particularly for a three-phase DAB, the effect of these unbalanced leakage impedances can be analytically determined and hence allowed for in the converter design process.

Since the two-level phase leg switching harmonics are referenced to the virtual neutral point of the three-phase coupling impedance network, the inter-bridge current for each phase can be independently solved analytically at each harmonic frequency using an equivalent single phase circuit. These individual harmonic current components can then be summed up again and the resultant overall current is evaluated to determine its zero crossing point, and hence whether ZVS is occurring for any particular DC bus operating voltage and PSSW phase shift angle $\delta$. Complex and non-ideal three-phase coupling impedances can be easily accommodated within the analysis approach, as well as the change in switching transition sequence that occurs between the primary and secondary bridges at a phase shift angle of +/- $60^\circ$. Furthermore, the approach can be applied to the problem of determining each phase leg’s ZVS condition for unbalanced transformer impedances caused by asymmetric location of the windings in relation to the high permeability magnetic path (i.e. the transformer core).

Fig. 4.1(a) shows the general structure of a three-phase DAB topology, where the primary and

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\(^1\)Material in this chapter was first published in:
Figure 4.1: Three-Phase DAB
secondary side converters are now connected via a general three-port admittance \([Y]\). An exemplar three-phase DAB coupling network is presented in Fig. 4.1(b), consisting of a high frequency three-winding transformer with primary and secondary series resistances and leakage inductances, and a central magnetising inductance. The three-phase legs of each bridge are switched with symmetrical 120° displacement, to generate a six-step output voltage pattern shown in Fig. 4.1(c). As with a single phase DAB, these patterns are then displaced by \(\delta\) to control the power transfer between the two bridges. Note that the symmetrical three-phase DAB switching pattern constrains the control of a basic three-phase DAB to a single control variable, unless a variable switch ON-state duty cycle (not constrained to 50%) is used as is well known from Pulse Width Modulation (PWM) theory [118] - [121].

4.1 Balanced Three-Phase Coupling Impedances

4.1.1 Fundamentals

For a three-phase DAB topology, the secondary bridge modulation is displaced by a phase angle \(\delta\) from the primary bridge for each corresponding phase \(z\) (\(z \in \{1, 2, 3\}\)). Hence the bridge phase leg harmonic voltages can now be expressed as follows:

\[
\begin{align*}
v_{p_z}(t) &= \frac{4V_{p, DC}}{\pi} \sum_{n=1}^{N} \frac{1}{m} \sin \left\{ m \left[ w_{sw} t - (z - 1) \cdot \frac{2\pi}{3} \right] \right\} \\
v_{s_z}(t) &= \frac{4V_{s, DC}}{\pi} \sum_{n=1}^{N} \frac{1}{m} \sin \left\{ m \left[ w_{sw} t - (z - 1) \cdot \frac{2\pi}{3} - \delta \right] \right\}
\end{align*}
\]

(4.1)

At each harmonic frequency, the bridge voltage components form either a positive \((m = 1, 7, 13 \ldots)\), negative \((m = 5, 11, 17 \ldots)\) or zero sequence \((m = 3, 9, 15 \ldots)\) balanced set of three-phase voltages. Since there is no fourth wire connection to the coupling impedance network from either bridge, the zero sequence (triplen) harmonic component sets cannot contribute to any current flow from either bridge, and hence can be discarded from (4.1) to result in the voltage pattern shown in Fig. 4.1(c). The remaining positive and negative sequence harmonic sets feed into the general three-phase network that couples between the two bridges. If this network is balanced, as shown in Fig. 4.1(b), each harmonic set can be analysed as a single phase equivalent circuit to determine the current flowing between the bridges at that harmonic frequency. These currents can then be summed to determine the overall inter-bridge current, which in turn can be analysed to find the ZVS conditions. Hence, the relationship between the primary and secondary bridge voltages and currents at each non-triplen harmonic frequency can be expressed using the generalised single phase two-port network relationship of

\[
\begin{bmatrix}
i^m_p(t) \\
i^m_s(t)
\end{bmatrix} =
\begin{bmatrix}
y^m_{p,p}(t) & y^m_{p,s}(t) \\
y^m_{s,p}(t) & y^m_{s,s}(t)
\end{bmatrix}
\begin{bmatrix}
v^m_p(t) \\
v^m_s(t)
\end{bmatrix}
\]

\((m \neq \text{triplen})\)

(4.2)

where \(y^m_{p,p}(t), y^m_{s,s}(t), y^m_{p,s}(t), y^m_{s,p}(t)\) are the self and mutual admittances at each harmonic frequency \(m\).
that couple the primary and secondary bridges. Substituting from (4.2), these (single phase equivalent) harmonic relationships can be alternatively expressed as a steady state phasor solution for each harmonic frequency, viz

\[
\begin{bmatrix}
I_{m,p}^p \\
I_{m,s}^s
\end{bmatrix}
= \begin{bmatrix}
Y_{m,p,p}^p \\
Y_{m,s,s}^s
\end{bmatrix}
\begin{bmatrix}
\frac{4V_{DC}}{\pi} \cos \frac{1}{m} \angle 0 \\
\frac{4V_{DC}}{\pi} \cos \frac{1}{m} \angle -m\delta
\end{bmatrix}_{(m \neq \text{triplen})}
\]

(4.3)

From this solution, the ZVS boundaries for the primary and secondary bridges can then be determined as follows:

\[
d|_{ZVS_p} \leq -\sum_{n=1}^{\infty} \frac{Y_{m,p}^p}{m} \left\{ \sin \left( \gamma_{m,p}^p \right) \cos \left( m\delta \right) - \cos \left( \gamma_{m,p}^p \right) \sin \left( m\delta \right) \right\}
\]

(4.4a)

\[
d|_{ZVS_s} \geq -\sum_{n=1}^{\infty} \frac{Y_{m,s}^s}{m} \left\{ \sin \left( \gamma_{m,s}^s \right) \cos \left( m\delta \right) + \cos \left( \gamma_{m,s}^s \right) \sin \left( m\delta \right) \right\}
\]

(4.4b)

For an ideal linear coupling inductance, these ZVS limits then become

\[
d|_{ZVS_p} = \frac{1}{d|_{ZVS_s}} \leq \frac{\sum_{n=1}^{\infty} \frac{1}{m^2}}{\sum_{n=1}^{\infty} \frac{\cos(m\delta)}{m^2}}
\]

(4.5)

Unfortunately in this form, (4.5) is not analytically solvable because of the explicit exclusion of the triplen harmonics, which creates a non-continuous summation series. However, it can be restated using continuous summation expressions and then solved taking into account periodicity and absolute value considerations for the two regions of |\delta| between (0 to \(\frac{\pi}{3}\)) and (\(\frac{\pi}{3}\) to \(\frac{\pi}{2}\)), to give

\[
d|_{ZVS_p} = \frac{1}{d|_{ZVS_s}} \leq \frac{2}{\sum_{n=1}^{\infty} \frac{1-\cos \left( m\frac{2\pi}{3} \right)}{m^2}}
\]

\[
= \begin{cases}
\frac{1}{1-\frac{\pi}{3m}} & \text{for } |\delta| \leq \frac{\pi}{3} \\
\frac{1}{2} & \text{for } \frac{\pi}{3} < |\delta| \leq \frac{\pi}{2}
\end{cases}
\]

(4.6)

Eqn. (4.6) exactly matches the results previously reported in [1].

4.1.2 Single Phase vs. Three-Phase

Fig. 4.2 illustrates how the ZVS boundary conditions vary for an ideal inductively coupled single phase and three-phase DAB with \(d\) and the PSSW phase shift angle \(\delta\) for both the closed form analytical solution and using a summation of harmonics. Fig. 4.2(a) shows the primary and secondary bridge ZVS boundaries for a single phase DAB with \(d\) as a function of \(\delta\), starting with the fundamental component...
only \((N = 1)\) and then with an increasing number of harmonics. The ZVS boundary curves clearly asymptote to the exact solutions of (3.11) as more harmonics are taken into account. From Fig. 4.2(b), it can be seen how the missing contribution of the triplen harmonics \((n = 2, 5, \text{ etc. leading to } m = 3, 9, \text{ etc.})\) reduces the ZVS range of a three-phase DAB compared to its single phase counterpart in the control range of \(|\delta| \leq 60^\circ\).

The number of harmonics that need to be considered to achieve a given ZVS accuracy can also be seen in Fig. 4.2. For a single phase DAB, as \(|\delta|\) heads towards \(\pi/2\), selecting only \(N = 2\) is sufficient to achieve an acceptable result. However at lower values of \(|\delta|\), more higher order harmonics need to be considered. For a three-phase DAB, the lack of triplen harmonic influence means that even \(N = 1\) still gives an acceptable ZVS prediction for higher values of \(|\delta|\). However, once again additional harmonics need to be taken into account as \(|\delta|\) reduces. Note that the controllable operating range of \(\delta\) is always practically limited from \(-\pi/2\) to \(\pi/2\) since these limits typically define the peak power flow boundaries.

### 4.1.3 ZVS Analysis for Non-Ideal AC Coupling Impedances

The ZVS analysis strategy for a balanced three-phase DAB system has been verified by matching theoretical, simulation and experimental investigations using balanced three-phase coupling networks that were built using individual coupled inductors (to minimise cross-coupling effects for simplicity) with a unity turns ratio.

Since the magnetising inductance of these coupled inductors is relatively large (as described in Chapter 9), they can be adequately modeled as a balanced \(RL\) impedance. The admittance matrix

<table>
<thead>
<tr>
<th>Imp.</th>
<th>(L(\mu\text{H}))</th>
<th>(R(\Omega))</th>
</tr>
</thead>
<tbody>
<tr>
<td>T1</td>
<td>252</td>
<td>1.2</td>
</tr>
<tr>
<td>T2</td>
<td>292</td>
<td>3.9</td>
</tr>
</tbody>
</table>

Table 4.1: Transformer series impedances (balanced three-phase DAB)
elements follow (3.13) and the ZVS boundaries reduce to

\[
d_{|ZVS_p} \leq \left| \sum_{n=1}^{\infty} \frac{1}{m} \{ \sin(\gamma_{m,p}^n) \} \right|_{(m \neq \text{triplen)}} \\
d_{|ZVS_s} \geq \left| \sum_{n=1}^{\infty} \frac{1}{m} \{ \sin(\gamma_{m,p}^n) \} \right|_{(m \neq \text{triplen)}} \tag{4.7a}
\]

Two impedance variations were considered, just the transformer alone (T1) with its internal AC winding resistance and leakage inductance, and a higher resistive alternative impedance (T2) where an additional (essentially resistive) impedance was added in series with the primary side winding. Table 4.1 lists the impedances of these two alternative coupling impedances T1 and T2. The switching frequency is 5 kHz (limited by the available experimental three-phase bridge).

Fig. 4.3(a) shows the effect of AC series resistance on the ZVS boundaries for these systems over the displacement angle \( \delta \). It can be derived that an increasingly resistive coupling impedance offsets the boundary conditions within which ZVS can occur - towards a lower DC bus ratio for positive power flow from the primary to secondary bridge (positive \( \delta \)), and towards a higher DC bus voltage ratio for positive power flow from the secondary to primary bridge (negative \( \delta \)), as already observed for the single phase DAB previously. Hence for example, at a DC bus voltage ratio \( d \) of 0.55 with positive power flow from primary to secondary, the secondary bridge will be operating in hard switching with T1, while it will still be operating with ZVS when T2 (higher resistance) is used. As shown in Fig. 4.3(a), since these offsets diverge depending on the direction of \( \delta \), they significantly constrain the DC bus voltage ratio conditions under which a single DAB system can operate in ZVS for both positive and negative values of \( \delta \).

Figs. 4.3(b) and 4.3(c) confirm this analysis with matching simulation and experimental results for T1 and T2. The figures show the primary and secondary bridge switched voltages and the primary phase 1 current. Recalling that the secondary phase current polarity is opposite to the primary phase polarity (for the case of an infinite magnetising inductance), Fig. 4.3(b) confirms that the secondary bridge operates in hard switching for \( d = 0.55 \) and \( \delta = \pi/6 \) with T1, but returns to soft switching conditions when T2 is substituted. Fig. 4.3(c) presents matching experimental results for this condition, with a 100 V primary DC bus voltage and a 55 V secondary DC bus voltage. Note that slight deviations in the current waveforms between the simulation and experimental results are caused by the frequency dependence of the physical transformer parameters and its actual finite transformer magnetising inductance (neglected in the simulation). These second order effects show the sensitivity of determining ZVS boundary conditions for more complex impedances.
4.2 Unbalanced Three-Phase Coupling Impedances

4.2.1 Fundamentals

To begin the analysis of unbalanced three-phase transformers, a fourth wire (virtual) neutral connection is added to both the primary and secondary sides in Fig. 4.1(b) to connect the transformer 'Y' star point voltages back to their respective DC link midpoint voltages. Fig. 4.4(a) presents a simplified representation of this arrangement, where the ideal three-phase coupling transformer has been eliminated because the mmf balance between the two sets of windings means that the two DC link midpoint voltages can be directly linked (with appropriate scaling of the secondary bridge voltages and currents for the transformer turns ratio) and the magnetising impedances shown in Fig. 4.1(b) are neglected for
simplicity of the analysis. This connection makes the phase currents \( i_{p,z,n}^{m} \) at each harmonic frequency \( m \) independent of each other and can be defined as follows:

\[
i_{p,z,n}^{m} = y_{p,z}^{m}(t)\{v_{p,z}(t) - v_{n}^{m}(t)\}, \quad z \in \{1, 2, 3\}
\]  

(4.8)

where \( y_{p,z}^{m}(t) \), \( y_{p2}^{m}(t) \), \( y_{p3}^{m}(t) \) are the unbalanced coupling impedances for each of the three phases. Note that (virtual) triplen harmonic currents can now flow in each phase current. Of course this connection also creates return harmonic current components through the neutral path given by

\[
i_{n}^{m}(t) = i_{p1,n}^{m}(t) + i_{p2,n}^{m}(t) + i_{p3,n}^{m}(t)
\]

(4.9)

An equal and opposite neutral compensating current \(-i_{n}^{m}\) is now injected into the three-phase system at each harmonic frequency \( m \) as shown in Fig. 4.4(b), which cancels the (virtual) neutral current created by the additional fourth wire neutral connection. This compensating current flows through each of the phase coupling impedances according to Kirchhoff’s current divider rule to give

\[
\begin{pmatrix}
  i_{n1}^{m}(t) \\
i_{n2}^{m}(t) \\
i_{n3}^{m}(t)
\end{pmatrix} =
\begin{pmatrix}
y_{p1,n}^{m}(t) \\
y_{p2,n}^{m}(t) \\
y_{p3,n}^{m}(t)
\end{pmatrix}\cdot
\begin{pmatrix}
  y_{p1,n}^{m}(t) & y_{p2,n}^{m}(t) & y_{p3,n}^{m}(t)
\end{pmatrix}
\]

(4.10)

where \( y_{p,n}^{m}(t) = y_{p1,n}^{m}(t) + y_{p2,n}^{m}(t) + y_{p3,n}^{m}(t) \). Using superposition to sum (4.8) and (4.10) and converting them to their equivalent phasor form in same way as was done for the balanced system analysis gives the actual phase currents of

\[
\begin{pmatrix}
  I_{p1}^{m} \\
  I_{p2}^{m} \\
  I_{p3}^{m}
\end{pmatrix} =
\begin{pmatrix}
  I_{p1,n}^{m} & I_{p2,n}^{m} & I_{p3,n}^{m}
\end{pmatrix}
\]

(4.11)

where

\[
Y_{p,z}^{m} \angle \gamma_{p,z}^{m} = Y_{p,z}^{m} \angle \gamma_{p,z}^{m} \left(1 - \frac{Y_{p2}^{m} \angle \gamma_{p2}^{m}}{Y_{p1}^{m} \angle \gamma_{p1}^{m}}\right) \quad Y_{p,y}^{m} \angle \gamma_{p,y}^{m} = -\frac{Y_{p,y}^{m} \angle \gamma_{p,y}^{m}}{Y_{p1}^{m} \angle \gamma_{p1}^{m}} \quad \forall \ z, y \in \{1, 2, 3\}, z \neq y
\]

(4.12)

and

\[
Y_{p1}^{m} \angle \gamma_{p1}^{m} = \frac{3}{R_{1} + jm\omega_{sw}L_{2}} \quad Y_{p2}^{m} \angle \gamma_{p2}^{m} = \frac{1}{R_{2} + jm\omega_{sw}L_{2}}
\]

(4.13)

If the two bridges are now modulated with balanced square wave modulation according to (4.1), the time varying form of the phase currents will not be balanced, and ZVS for each of the three phases will not occur at the same values of \( d \) and \( \delta \). Hence the ZVS region for the overall converter will be reduced to that of the first phase current to reach its ZVS boundary irrespective of the switching
conditions of the other two phases, and this will constrain the ZVS operation range of the DAB. Also note that hard switching of one phase leg only inevitably creates a phase shift deviation of this inverter leg output voltage with respect to the other (soft switched) inverter legs, which may further unbalance the switching conditions.

To address this limitation, the primary and secondary bridge switched voltages are now deliberately phase shifted away from their previous symmetric 120° displacement, to compensate for the unbalanced coupling impedances as illustrated by Fig. 4.5. Under these conditions, the bridge voltages are defined in time domain by the following series of harmonic voltage component summations:

\[
\begin{align*}
v_{p1}(t) &= \frac{4V_{p,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{m} \sin \{m[w_{m}t]\} \\
v_{p2}(t) &= \frac{4V_{p,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{m} \sin \{m[w_{m}t - 2\pi/3 - \nu_{p2}]\} \\
v_{p3}(t) &= \frac{4V_{p,DC}}{\pi} \sum_{n=1}^{N} \frac{1}{m} \sin \{m[w_{m}t - 4\pi/3 - \nu_{p3}]\}
\end{align*}
\]

where \(\nu_{p2}, \nu_{p3}, \nu_{s2}, \nu_{s3}\) are the additional arbitrary selected compensation angles that have been introduced to modify the primary and secondary bridge switched voltages to compensate for the unbalanced coupling impedances. As can be seen from the equations, only the phase shift between the bridge phase legs of phase 1 (set as reference) remains \(\delta\), while the absolute phase shifts between the bridge legs of phase 2 and phase 3 can be larger or lower than \(\delta\). It is also commented that the triplen harmonic contribution in (4.14) is not zero any further and must now to be taken into account when determining the ZVS boundary conditions.

Using the same approach as for the balanced impedance system, (4.14) can now be converted into phasor form and substituted into (4.11) to create deterministic phasor expressions for the current flowing in each phase at each harmonic frequency \(m\). These phasor expressions can then be converted back into time domain form and summed to achieve an overall time domain form for each phase current of (phase 1 of the primary bridge only shown)

\[
\begin{align*}
\sum_{n=1}^{N} \frac{1}{m} \sin \{m[w_{m}t - \delta]\} \\
\sum_{n=1}^{N} \frac{1}{m} \sin \{m[w_{m}t - 2\pi/3 - \delta - \nu_{p2}]\} \\
\sum_{n=1}^{N} \frac{1}{m} \sin \{m[w_{m}t - 4\pi/3 - \delta - \nu_{p3}]\}
\end{align*}
\]

Figure 4.5: ZVS compensation angles for unbalanced three-phase DAB
An example three-phase DAB converter switching at 5 kHz with total transformer leakage inductances of $L_1 = L_3 = 250 \mu H$, $L_2 = 0.6L_1$ and negligibly small AC resistances ($R_1 = R_2 = R_3 = 0.1 \Omega$) is now used to illustrate the impact of impedance unbalance on the converter ZVS boundaries. Under these impedance conditions, Fig. 4.6(a) shows the primary (upper) and secondary (lower) ZVS boundaries for the three phase legs of each bridge as the PSSW displacement angle $\delta$ varies, with symmetric three-phase switched voltages for each bridge (i.e $\nu_{p2} = \nu_{p3} = \nu_{s2} = \nu_{s3} = 0$). For power transfer from primary-to-secondary ($\delta > 0$) and $d > 1$, the ZVS boundary of primary bridge phase leg 1 ($d_{ZVS_{p1}}$) moves down while the ZVS boundary of primary bridge phase leg 2 moves up as the leakage inductance on phase leg 2 is progressively decreased with respect to the other two phases (note that the opposite happens for a secondary-to-primary power transfer, i.e. $\delta < 0$). Hence, for operation with
an unbalanced three-phase transformer impedance, for $\delta > 0$ and $d > 1$, the ZVS region for the overall converter is constrained to the $d|_{ZVS_{p_1}}$ boundary, irrespective of the switching conditions of the other two phases. A similar response occurs for the $d|_{ZVS_{p_3}}$ boundary when power transfers in the reverse direction.

Similar ZVS restrictions occur for the secondary bridge when the converter operates at $d < 1$. For $\delta > 0$, the ZVS boundary of secondary bridge phase leg 1 ($d|_{ZVS_{s_1}}$) moves down while the ZVS boundary of secondary bridge phase leg 3 ($d|_{ZVS_{s_3}}$) moves up as the leakage inductance on phase leg 2 is progressively decreased with respect to the other two phases (the opposite happens for $\delta < 0$). Hence, for operation with an unbalanced three-phase transformer impedance, for $\delta > 0$ and $d < 1$, the ZVS region for the overall converter is constrained to the $d|_{ZVS_{s_3}}$ boundary, irrespective of the switching conditions of the other two phases. A similar response occurs for the $d|_{ZVS_{s_1}}$ boundary when power transfers in the reverse direction.

To have a more specific example, the harmonic solution predicts that when $\delta = \frac{\pi}{6}$, the secondary bridge third phase leg limits the ZVS switching range to $d = 0.83$ as shown in Fig. 4.6(a). Using a simulation environment (primary DC bus voltage: 100 V), Fig. 4.6(b) shows the simulated phase current waveforms and the secondary bridge (top-side) gate signals for a further reduced DC-DC conversion ratio of $d = 0.74$ with a primary-side DC bus voltage of 100 V. Since all secondary bridge currents have to be negative to ensure ZVS, the third phase of the secondary bridge is clearly operating outside ZVS because $i_{s,3}(t) = -i_{p,3}(t)$ is positive for the negative-to-positive voltage transition of this phase leg. In contrast, as also predicted by the analysis solution in Fig. 4.6(a), the other two secondary bridge phase currents are negative (or zero) and hence these phase legs are operating within ZVS at this phase displacement angle and bridge voltage ratio.
4.2. UNBALANCED THREE-PHASE COUPLING IMPEDANCES

4.2.3 Asymmetrical Modulation

The four additional compensation angles $\nu_{p2}$, $\nu_{p3}$, $\nu_{s2}$, $\nu_{s3}$ can now be used as independent degrees of freedom to dynamically compensate for the effect of three-phase unbalanced interconnecting impedances.

Fig. 4.7 exemplarily illustrates the individual influence of the selected compensation angles $\nu_{p2}$ and $\nu_{p3}$ (steps of $\pm$ 0.2 rad, $\nu_{s2} = \nu_{s3} = 0$) on the three primary bridge ZVS boundaries for $d > 1$ and a balanced three-phase transformer impedance. From Fig. 4.7(a), for $\delta > 0$, primary bridge phase leg 1 is the most limiting for ZVS operation, and $\nu_{p2} > 0$ and/or $\nu_{p3} < 0$ can be used to alleviate this limitation. For $\delta < 0$, ZVS is mostly limited by the primary bridge phase leg 3, and $\nu_{p2} < 0$ and/or $\nu_{p3} > 0$ are capable of extending the ZVS operation. Fig. 4.8 illustrates the individual influence of the compensation angles $\nu_{s2}$ and $\nu_{s3}$ ($\nu_{p2} = \nu_{p3} = 0$) on the three secondary bridge ZVS boundaries for $d < 1$ and a balanced three-phase transformer impedance. From Fig. 4.8(a), for $\delta > 0$, secondary bridge phase leg 3 is the most limiting for ZVS operation, and $\nu_{s2} < 0$ and/or $\nu_{s3} > 0$ contribute to mitigate this limitation. For $\delta < 0$, ZVS is mostly limited by the primary bridge phase leg 1, and $\nu_{s2} > 0$ and/or $\nu_{s3} < 0$ can be used to extend the ZVS operation.

As for the previous example, when the symmetric three-phase primary bridge output voltages are now intentionally unbalanced by applying $\nu_{p2} = 0.044$ rad and $\nu_{p3} = -0.150$ rad, the ZVS conditions for the secondary bridge can be exactly matched at $\delta = \frac{\pi}{6}$ to achieve ZVS soft switching for a minimum
conversion ratio of \( d = 0.74 \) as shown in Fig. 4.9(a). The simulated current waveforms are shown in Fig. 4.9(b), where, as predicted by the analytical model, all phase legs of the secondary bridge are now soft switched since all phase currents reach zero (the theoretical ZVS boundary) at the negative-to-positive phase leg voltage transition (i.e. turn-ON of the high side devices). It should also be noted in Fig. 4.9(b) that the peak current amplitudes and average power transfer per phase are now (implicitly) more balanced, which is an additional side benefit of the asymmetrical voltage switching of each phase leg.

![Diagram](image_url)

**Figure 4.8:** Effect of secondary bridge compensation angles on secondary bridge ZVS limits over \( \delta \) for balanced three-phase inductive impedance and \( d < 1 \)

![Diagram](image_url)

**Figure 4.9:** Asymmetric Modulation of unbalanced three-phase DAB (\( \nu_{p2} = 0.044, \nu_{p3} = -0.150 \) rad)
4.2. UNBALANCED THREE-PHASE COUPLING IMPEDANCES

Figure 4.10: Dynamic adaption of secondary bridge ZVS boundaries for unbalanced three-phase DAB

Applying these principles to an application example with operating conditions close to the previous simulation example (primary DC bus voltage: 100 V, operating frequency: 5 kHz), Fig. 4.10 now illustrates how the phase angle $\nu_{s3}$ alone can be used to shape the secondary bridge boundaries to extend the overall converter ZVS range for $\delta > 0$ with a required minimum conversion ratio of $d = 0.81$.

For a specific balanced three-phase and non-ideal resistive transformer impedance (parameters: $L_1 = L_2 = L_3 = 250 \mu H$ and $R_1 = R_2 = R_3 = 1.2 \Omega$), Fig. 4.10(a) shows that the minimum (main) displacement angle for ZVS operation is $\delta = 0.31$ rad, while from Fig. 4.10(b), for a given unbalanced three-phase transformer (parameters: $L_1 = L_3 = 250 \mu H$, $L_2 = 0.6L_1$, $R_1 = R_3 = 1.2 \Omega$, $R_2 = 0.67R_3$) using symmetrical modulation, complete ZVS operation is only possible for $\delta \geq 0.425$ rad. However, by intentionally implementing an asymmetrical converter modulation pattern with $\nu_{s3}$ set according to the characteristic shown in Fig. 4.10(b), the same ZVS range capability as for the DAB with a balanced three-phase coupling impedance can also be achieved for the unbalanced impedance scenario.

These theoretical concepts have been experimentally verified using balanced and unbalanced three-phase coupling impedances constructed with individual coupled-inductors with a unity turns ratio. Impedance unbalance was implemented by reducing the number of turns on both windings of the phase 2 coupled-inductor by about one third. The DAB converter was operated with a voltage ratio $d = 0.81$ and phase shifts $\delta = \{0.32, 0.373, 0.425\}$ rad, with the compensation angle $\nu_{s3}$ adjusted manually. Fig. 4.11(a) shows experimental secondary bridge phase currents and switched phase leg voltages (with respect to the secondary-side negative DC bus rail) for a balanced three-phase coupling impedance, a symmetrical modulation pattern and a phase shift angle of $\delta = 0.32$ rad. From Fig. 4.11(a), despite the small practical three-phase impedance unbalance, all three phases operate in ZVS (i.e. $i_{p1} = -i_{s1} > 0$ during a positive transition in $\nu_{s1-o}$, and same outcomes for phases 2 and 3).
Fig. 4.11(b) presents matching experimental results for the introduced unbalanced three-phase transformer impedance where the converter is again modulated with the same symmetrical PSSW modulation pattern. Under these conditions, phases 1 and 2 operate in ZVS (i.e. \( -i_{s1} > 0 \) for a positive \( v_{s1-0} \) transition and \( -i_{s2} > 0 \) for a positive \( v_{s2-0} \) transition). However, as anticipated from Fig. 4.10(b), phase leg 3 becomes hard switched (\( -i_{s3} < 0 \) for a rising \( v_{s3-0} \) transition).

Figure 4.12: Experimental waveforms of three-phase DAB currents for unbalanced three-phase impedance and asymmetrical modulation
Fig. 4.12 presents further experimental results for the same unbalanced three-phase coupling impedance, where the converter is now modulated with an asymmetrical pattern. Fig. 4.12(a) shows experimental phase currents for operation with angles $\delta = 0.32$ rad, $\nu_{s3} = 0.09$ rad (i.e. operating point OP1 from Fig. 4.10(b)). Under those conditions, secondary bridge phase leg 3 now operates just within the ZVS boundary range (i.e. $-i_{s3} > 0$ for a positive $v_{s3-0}$ transition), while phase legs 1 and 2 comfortably operate with ZVS. From Fig. 4.12(b), for a larger power transfer at phase shift $\delta = 0.37$ rad, angle $\nu_{s3}$ is now set to 0.045 rad (OP2 in Fig. 3.10(b)) to again allow all converter phase legs to operate with ZVS. Finally, from Fig. 4.12(c), for a further increase in power transfer with $\delta = 0.425$ rad, phase angle $\nu_{s3}$ can be set back to zero (OP3 in Fig. 4.10(b)) since secondary bridge phase 3 no longer limits ZVS operation under symmetrical modulation.

4.3 Summary

This chapter has shown how to extend the ZVS boundary analysis from Chapter 3 into a similar solution expression for a balanced three-phase DAB, by exclusion of triplen harmonics. These results can again be used to accurately determine the ZVS boundaries for any particular DAB design and operating context, where numerical integration has been used to illustrate how complex bridge coupling networks influence the ZVS boundary conditions. For an unbalanced three-phase DAB transformer, the available overlapping ZVS region across the three phase legs of each bridge has been illustrated to shrink since the boundary conditions for each phase leg now differ. In this context, it has also been shown how asymmetric three-phase modulation patterns can be used to regain ZVS operating range.
5 Maintaining Continuous ZVS Operation by Advanced Transformer Design and Adaptive 3-Level Modulation

It is well known that to maintain high conversion efficiency, a DAB should preferably operate under soft switching conditions across its entire operating range. Indeed, promising switching technologies such as super-junction FET [122] or wide bandgap devices such as GaN [30], which have an outstanding ZVS soft switching performance, cannot be utilized at their best capability unless ZVS conditions can be guaranteed under all steady-state operating conditions. Furthermore, since the controllability of a DAB is adversely affected by the transition from ZVS to hard switching when dead-time is significant [96] [98] [116], it is desirable to avoid this transition from a control perspective.

A DAB is typically controlled using 2-level Phase Shifted Square Wave (PSSW) modulation [1]. However, to extend the ZVS capability of a DAB across a wider range of DC-DC bus voltage ratios, 3-level PSSW modulation can be used to create a variable volt-second bridge output [35] [37]. Various strategies such as dual phase shift modulation [36], triple phase shift control [38], triangular/trapezoidal modulation [39] and hybrid modulation [43] have been proposed to achieve this result, essentially using the same three degrees of control freedom of primary and secondary bridge duty cycles, and the phase shift between the two bridge switched voltage outputs. However, independent of the modulation scheme used, second-order switching device non-idealities such as dead-time and device capacitances prevent continuous ZVS operation being achieved across some parts of the DAB target operating range if the magnetising current is not explicitly included into the design process, leading to a simplified series inductance modeling technique [50] [56] [57] [58] [104]. Irrespective of the size of this transformer leakage (and/or externally added) inductance, hard switching always occurs when the primary and secondary bridge phase leg transitions overlap, unless additional circulating current is created by including additional AC link components [60] [123] [124] or other auxiliary hardware circuits [125] that tend to reduce the DAB power density.

The frequency domain analysis presented in Chapter 3 has identified precise ZVS boundary condi-

\[1\] Material in this chapter was first published in:
5.1 ZVS LIMITATIONS FOR PRACTICAL DAB DC-DC CONVERTERS

Figure 5.1: Single Phase DAB topology and HF transformer circuit model

tions of a DAB under all operating conditions, including the use of 3-level PSSW modulation, complex coupling impedances [126] and taking into account the major switching non-idealities of phase leg dead-time and device capacitances. This chapter now uses this approach to determine the DAB transformer parameters that allow a DAB to continuously operate in ZVS under all designed operating conditions. The work begins by identifying the inevitable hard switching regions that occur for a DAB using a conventional AC link series impedance analysis approach when dead-time and device capacitance are taken into account [110]. Previous work [39] has already identified how an increased transformer magnetising current can increase the ZVS region of a DAB. Harmonic analysis is then used to determine the AC link transformer parameters of magnetising inductance and leakage inductances in Fig. 5.1 that allow the DAB to operate in ZVS over its entire operating range, while taking dead-time and device capacitances into account. Such an analysis is required to determine the minimum necessary magnetising current that still maintains the required ZVS operating range using adaptive 3-level PSSW modulation, i.e. design for as large a magnetising inductance as possible, to limit the (inevitable) increase of DAB conduction losses as much as possible.

Fig. 5.2(a) shows the ZVS boundaries for a DAB modelled with a simple series AC link inductance (i.e. infinite transformer magnetising inductance) and controlled by 2-level PSSW modulation. Under these conditions, the ZVS region has a cusp at the zero power transfer point (i.e. $\delta = 0$), which means that the converter can only maintain ZVS when passing through this point for an exactly nominal unity DC-DC bus voltage ratio ($d=1$) which is quite unlikely in practice. Figs. 5.2(b)-(c) show how this cusp then disappears when minimum ZVS commutation current (device capacitance) and dead-time effects are considered, creating a region at low power transfer levels where ZVS simply cannot be maintained.

Fig. 5.2(d)-(f) show the effect of reducing the transformer magnetising inductance $L_m$ from infinity...
CHAPTER 5. MAINTAINING CONTINUOUS ZVS OPERATION

Figure 5.2: ZVS boundaries for conventional 2-level DAB modulation ($\alpha = \beta = \pi$) with constant transformer leakage inductances. (a)-(c): Infinite magnetising inductance (coupling factor: $k_T = 1.0$), (d)-(f): Reduced magnetising inductance (coupling factor: $k_T = 0.8$)

Figure 5.3: ZVS boundaries for adaptive 3-level DAB modulation of one bridge (example: $\alpha = \pi/2, \beta = \pi$) with constant transformer leakage inductances. (a)-(c): Infinite magnetising inductance (coupling factor: $k_T = 1.0$), (d)-(f): Reduced magnetising inductance (coupling factor: $k_T = 0.8$)

so that the winding coupling factor $k_T = \frac{L_m}{\sqrt{(L_m+L_{\sigma,p})(L_m+L_{\sigma,s})}}$ reduces to 0.8, while keeping the winding leakage inductances $L_{\sigma,p}$ and $L_{\sigma,s}$ constant and equal. In practice, this design change can be achieved by making the core airgap larger than the minimum value which is required to manage DC flux generation caused by the transient and steady-state switching processes. This creates a beneficial circulating current
that increases the ZVS range of the DC-DC bus voltage ratio for any phase shift angle. Fig. 5.2(d) shows this effect, where the upper and lower ZVS boundaries vertically diverge and create a ZVS “channel” through the zero power transfer point which allows continuous ZVS operation to be maintained for DC-DC voltage ratios that vary away from unity. Figs. 5.2(e)-(f) show that while this channel narrows and skews when switch device capacitance and dead-time are taken into account, the DAB can still continuously operate under ZVS conditions as the power transfer level passes through zero, for a useful practical range of off-nominal DC bus voltage ratios.

Figs 5.3(a)-(c) show how 3-level modulation affects the ZVS boundaries for the same ideal series inductance model. Firstly, Fig. 5.3(a) shows how a 3-level modulated primary bridge splits the 2-level single ZVS cusp into two cusp points, located $\delta = \pm \frac{1}{2} |\alpha - \beta|/2$ away from the zero power transfer point of $\delta = 0$, and centred around a DC-DC bus voltage ratio of $d = 0.5$, since $\alpha = \frac{\pi}{2}$ in this example (these cusp points can of course can be moved up or down to suit any actual DC-DC bus voltage ratio by appropriate selection of $\alpha$ for $d < 1$ and $\beta$ for $d > 1$, accordingly to the relationship $d = \alpha/\beta$). Figs. 5.3(b)-(c) then show how these dual cusps similarly disappear once non-ideal switching effects are taken into account, once again creating regions of power transfer where ZVS simply cannot be maintained.

When the magnetising inductance is reduced for 3-level modulation in the same way as for 2-level modulation before, the ZVS boundaries again vertically diverge to create a ZVS channel across the entire power transfer range, as shown in Fig. 5.3(d) for a transformer coupling factor of $k_T = 0.8$. Figs 5.3(e)-(f) show how this channel narrows when device capacitances are accounted for, and then pinches (for this example) when dead-time effects are also included to a point where only one singular horizontal ZVS path remains at a particular value of $d$, for constant values of $\alpha$ and $\beta$.

The conclusion from this analysis is that two steps are required to achieve continuous ZVS operation of a DAB over its entire operating range. Firstly, the transformer magnetising inductance must be reduced sufficiently (by design) to create an adequate ZVS “channel” throughout the power transfer range, taking into account both device capacitance and dead-time effects. Secondly, the 3-level modulation duty cycles of $\alpha$ and $\beta$ must be varied during DAB operation to place this channel to match the actual DC-DC bus voltage ratio that exists at any particular point in time and for any particular power operating level.

5.2 Determining the Required Reduction in Magnetising Inductance

Increasing the circulating current in a DAB has the potential to increase the overall converter losses. Hence the challenge now is to determine the minimum reduction in magnetising inductance that is required to achieve continuous ZVS operation across the entire DAB designed operating range (i.e. $\delta \in [0, \pi/2]$, $d_{\text{min}} \leq d \leq d_{\text{max}}$).
CHAPTER 5. MAINTAINING CONTINUOUS ZVS OPERATION

To simplify the analysis, the transformer inductances are now assumed to be frequency independent and the winding resistances are neglected (these can be quite realistic assumptions as shown in Table 6.1 and 6.2 for the experimental transformer). The transformer model in Fig. 5.1 then reduces to three parameters: the total winding leakage inductance \( L \), the leakage inductance split between the primary and secondary winding \( \chi \) and the transformer coupling co-efficient \( k_T \). From fundamental transformer theory, these parameters are related as follows:

\[
L_\sigma, p = \chi L \quad L_\sigma, s = (1 - \chi)L \quad k_T = \frac{L_m}{\sqrt{(L_m + L_\sigma, p)(L_m + L_\sigma, s)}} \tag{5.1}
\]

Rearranging from (5.1), the magnetising inductance can then be expressed as

\[
L_m = \frac{L \cdot k_T^2}{2(1 - k_T^2)} + L \cdot k_T \sqrt{\frac{k_T^2}{4(1 - k_T^2)^2} + \frac{(1 - \chi)\chi}{1 - k_T^2}} = \frac{k_T \cdot L}{2(1 - k_T^2)} \bigg|_{\chi=0.5} \tag{5.2}
\]

However, to remove the dependency of \( L_m \) on \( \chi \) in (5.2), a modified coupling co-efficient \( K \) is now defined, so that

\[
L_m = \frac{K \cdot L}{2(1 - K)} \tag{5.3}
\]

for any value of leakage inductance split between the two windings. Fig. 5.4 shows the equivalent transformer model to Fig. 5.1(a) using these inductance simplifications and relationships.

Using this reduced transformer model, the generalised two-port AC link admittance elements in (3.4) become

\[
Y_{m, p}^m \angle \gamma_{m, p}^m = \frac{1}{mL_{sw}} \cdot \frac{K + 2(1 - \chi)(1 - K)}{K + 2\chi(1 - \chi)(1 - K)} \angle -\frac{\pi}{2}
\]

\[
Y_{m, s}^m \angle \gamma_{m, s}^m = \frac{1}{mL_{sw}} \cdot \frac{K + 2\chi(1 - K)}{K + 2\chi(1 - \chi)(1 - K)} \angle -\frac{\pi}{2}
\]

\[
Y_{p, s}^m \angle \gamma_{p, s}^m = Y_{p, s}^m \angle \gamma_{p, s}^m = \frac{1}{mL_{sw}} \cdot \frac{K}{K + 2\chi(1 - \chi)(1 - K)} \angle \frac{\pi}{2}
\]

which can then be used to determine the largest value of \( K \) that allows the DAB to continuously operate in ZVS across its entire operating range.

Figure 5.4: Lossless DAB transformer model
5.2.1 2-Level Modulation

Substituting (5.4) into (3.7), and controlling the DAB with 2-level PSSW modulation by setting \( \alpha = \beta = \pi \), the ZVS boundary conditions with ideal switching devices become

\[
d_{\text{ZVS}_s} = d_{\text{ZVS}_p} = \frac{K}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)]} \left[ \sum_{n=1}^{\infty} \frac{\cos(m\delta)}{m^2} \right] \frac{\pi - 2|\delta|}{\pi} (5.5a)
\]

\[
d_{\text{ZVS}_s} = \frac{K+2(1-\chi)(1-K)}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)]} \left[ \sum_{n=1}^{\infty} \frac{1}{m^2} \right] \frac{\pi - 2|\delta|}{\pi} (5.5b)
\]

Note the reduction of the infinite harmonic summation to a more compact explicit analytical form in this expression. Next, a minimum circulating current of \( \Delta i_p \) for the primary bridge and \( \Delta i_s \) for the secondary bridge needs to be included into (5.5) to account for switching device capacitance, which gives revised ZVS boundary conditions of

\[
d_{\text{ZVS}_s} \geq \frac{K}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)]} \left[ \sum_{n=1}^{\infty} \frac{\cos(m\delta)}{m^2} \right] + \frac{\pi \Delta i_s}{8 \pi \delta_{p,\text{DC}}} = \frac{K(\pi-2|\delta|) + \Delta i_s}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)] K+2x(1-\chi)(1-K) \pi} \quad |\delta| \leq \pi (5.6a)
\]

\[
d_{\text{ZVS}_s} \leq \frac{K+2(1-\chi)(1-K)}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)]} \left[ \sum_{n=1}^{\infty} \frac{1}{m^2} \right] + \frac{\pi \Delta i_p}{8 \pi \delta_{p,\text{DC}}} = \frac{K+2(1-\chi)(1-K)}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)] K+2x(1-\chi)(1-K) \pi} \quad |\delta| \leq \pi (5.6b)
\]

Lastly, the influence of dead-time needs to be incorporated into (5.6) by adding the dead-time phase angle shifts as per (3.15), using \( r = 1 \) as the worst case, to the admittance elements of (3.4). Note that only the primary bridge dead-time angle \( \rho_{\text{DT}_p} \) needs to be added for the positive power flow region (\( \delta \geq 0 \)) and only the secondary bridge dead-time angle \( \rho_{\text{DT}_s} \) needs to be added for the negative power flow region (\( \delta \leq 0 \)), since these are the particular dead-times that reduce the available ZVS region. This leads to the final practical ZVS boundary definitions of (as compared to (3.18))

\[
d_{\text{ZVS}_s} \geq \frac{K}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)]} \left[ \sum_{n=1}^{\infty} \frac{\cos(m\delta+\rho_{\text{DT}_s})}{m^2} \right] + \frac{\pi \Delta i_s}{8 \pi \delta_{p,\text{DC}}} + \frac{\Delta i_s}{8 \pi \delta_{p,\text{DC}}} \quad \frac{K(\pi-2|\delta+\rho_{\text{DT}_s}|)}{w_{\text{sw}} L_{\text{K}} [K+2x(1-\chi)(1-K)] K+2x(1-\chi)(1-K) \pi} \left( 1 + \frac{2\rho_{\text{DT}_s}}{\pi} \right) (5.7a)
\]

Figure 5.5: Cusp operating conditions for 2-level modulation
As shown in Fig. 5.2(f), the most constrained ZVS operating point for 2-level modulation occurs at the cusp points where \( \delta = \rho_{DT_p} \) for positive power flow, and \( \delta = -\rho_{DT_s} \) for negative power flow. Hence to maintain continuous ZVS operation, these cusp points must be located outside the DC-DC bus voltage ratio design limits \( (d_{\text{min}} \text{ and } d_{\text{max}}) \), i.e.

\[
\begin{align*}
\left| d_{\text{ZVS}_{p(cusp)}} \right| &= \frac{K \pi + 2\pi(1-\chi)(1-K) \sum_{n=1}^{\infty} \cos\left(\frac{m\pi DT_L}{T_{p,\text{DC}}} \right)}{w_{sw} L[K + 2\chi(1-\chi)(1-K)] \sum_{n=1}^{\infty} \cos\left(\frac{m\pi DT_L}{T_{p,\text{DC}}} \right)} \leq d_{\text{min}} \quad (5.8a) \\
\left| d_{\text{ZVS}_{p(cusp)}} \right| &= \frac{K \pi + 2\pi(1-\chi)(1-K) \sum_{n=1}^{\infty} \cos\left(\frac{m\pi DT_L}{T_{p,\text{DC}}} \right)}{w_{sw} L[K + 2\chi(1-\chi)(1-K)] \sum_{n=1}^{\infty} \cos\left(\frac{m\pi DT_L}{T_{p,\text{DC}}} \right)} \geq d_{\text{max}} \quad (5.8b)
\end{align*}
\]

Rearranging (5.8) identifies the required modified coupling co-efficient \( K \) that can achieve this objective, i.e.

\[
\begin{align*}
K \bigg|_{d_{\text{min}}} &= \frac{d_{\text{min}}(1 + \frac{2\rho_{DT_L}}{\pi})2\pi - \frac{\Delta_{I_p}}{T_{p,\text{DC}}} L[2\chi(1 - \chi)]}{\pi + \frac{\Delta_{I_p} w_{sw} L}{T_{p,\text{DC}}}[1 - 2\chi(1 - \chi)] - \frac{\Delta_{I_p}}{T_{p,\text{DC}}} L[2\chi(1 - \chi)]} \quad (5.9a) \\
K \bigg|_{d_{\text{max}}} &= \frac{2\pi(\chi - 1)(1 - \frac{2\rho_{DT_L}}{\pi}) + \frac{\Delta_{I_p} w_{sw} L}{T_{p,\text{DC}}}[2\chi(1 - \chi)]}{1 - 2(1 - \chi)\pi(1 - \frac{2\rho_{DT_L}}{\pi}) - \frac{\Delta_{I_p} w_{sw} L}{T_{p,\text{DC}}}[2\chi(1 - \chi)] - d_{\text{max}}\pi} \quad (5.9b)
\end{align*}
\]

The overall maximum possible value of \( K \) is the smaller of the two values determined by (5.9a) and (5.9b), viz:

\[
K^{\text{ZVS}}_{\text{max}} = \min \left\{ K \bigg|_{d_{\text{min}}}, K \bigg|_{d_{\text{max}}} \right\} \quad (5.10)
\]

Fig. 5.6(a) shows \( K^{\text{ZVS}}_{\text{max}} \) required to maintain continuous ZVS operation as the DC-DC bus voltage ratio \( d \) varies, when switching device capacitance and dead-time are not considered. Two curves are shown, one for an equal winding split of \( \chi = 0.5 \), and the other one for an actual leakage winding split of \( \chi = 0.67 \), to match the physical transformer used for the experimental work described in Chapter 6.

Fig. 5.6(b) then shows \( K^{\text{ZVS}}_{\text{max}} \) over \( d \) when switch device capacitance and dead-time (values as listed in Table 6.3) are taken into account for \( L = 3.35 \) \( \mu \text{H} \) (Table 6.2). The reduction in \( K^{\text{ZVS}}_{\text{max}} \) that is necessary to maintain ZVS over any specified DAB operating range for \( d \) when these second order effects are taken into account, which translates directly to a decreased magnetising inductance and an increased magnetising current, is clearly visible.
5.2. Determining the Required Reduction in Magnetising Inductance

5.2.2 Adaptive 3-Level Modulation of One Bridge

Minimum DC-DC Bus Voltage Ratio

Fig. 5.3 shows how for a reduced DC-DC bus voltage ratio \( d < 1 \), the primary bridge duty cycle \( \alpha \) can be reduced to move the low power transfer ZVS region down to match this ratio. However, this also splits the single ZVS cusp point created by 2-level modulation, into two cusp points that are displaced away from the zero power transfer point at \( \delta = 0 \) by \( \delta = \pm |\alpha - \beta|/2 \). Fig. 5.3(f) shows how the ZVS channel created with this modulation strategy then pinches to a singular horizontal path in the positive power transfer region when device capacitance and dead-time are considered. The challenge now is to find the values of \( K \) and \( \alpha \) that define this minimum continuous ZVS path condition.

Mathematically, this limiting condition can be identified as when the lower of the two values of \( d \) at the cusps of the primary bridge (HB1 and HB2) ZVS boundaries is the same as the higher of the two values of \( d \) at the cusps of the secondary bridge (HB3 and HB4) ZVS boundaries, and also equals the minimum designed bus voltage ratio \( d_{\text{min}} \), i.e.

\[
d^{\text{ZVS}_{p,\text{ZVS}}} = d_{\text{min}} = d^{\text{ZVS}_{s,\text{ZVS}}}
\] (5.11)

Under these conditions, \( \alpha \in [0,\pi] = \alpha_{\text{cusp}} \) and \( \beta = \pi \) (note that \( \beta \) typically equals \( \pi \) for a DC bus voltage ratio of less than unity). Furthermore, only the cusp points for HB1 and HB3/HB4 need to be considered for operation in the positive power transfer region (\( \delta \geq 0 \)), since these phase legs always have the closest two cusp points (similarly, only the cusp points for HB2 and HB3/HB4 need to be considered for operation in the positive power transfer region).

Figure 5.6: ZVS design requirement of coupling co-efficient for conventional 2-level PSSW modulation

Figure 5.7: Exemplar cusp operating condition at \( d_{\text{min}} (\alpha = \alpha_{\text{cusp}}) \)
when \( \delta < 0 \).

Substituting (5.4) into (3.18) defines the ZVS operating boundaries for a DAB with a reduced coupling factor transformer used as the AC link impedance, with the cusp points occurring at

\[
\delta_p = \frac{\alpha_{\text{cusp}} - \beta}{2} + \rho_{\text{DT}_p} \quad \text{for HB1} \tag{5.12a}
\]

\[
\delta_n = \frac{\alpha_{\text{cusp}} - \beta}{2} \quad \text{for HB3 and HB4} \tag{5.12b}
\]

recognising that the secondary bridge dead-time has no influence on ZVS operation in this power region.

Reflecting also from (5.11) into the revised 3.18(a) and 3.18(d) then gives, with some manipulation, ZVS DC bus voltage ratio boundary limits at these cusp points of

\[
d_{\text{min}} = \frac{\frac{K\pi}{w_{\text{op}} L[K + 2\chi(1 - \chi)]} \sum_{n=1}^{\infty} \frac{8\sin^2(m\alpha_{\text{cusp}}/2)}{\pi^2 m^2} \sum_{m=1}^{\infty} \frac{8}{\pi^2 m^2}}{\sum_{n=1}^{\infty} \frac{8\sin^2(m\alpha_{\text{cusp}}/2)}{\pi^2 m^2}} + \frac{\Delta_{\text{ip}}}{V_{\text{p,DC}}}
\]

\[
d_{\text{min}} = \frac{\frac{K\pi}{w_{\text{op}} L[K + 2\chi(1 - \chi)]} \sum_{n=1}^{\infty} \frac{8\sin^2(m\alpha_{\text{cusp}}/2)}{\pi^2 m^2} \sum_{m=1}^{\infty} \frac{8}{\pi^2 m^2}}{\sum_{n=1}^{\infty} \frac{8\sin^2(m\alpha_{\text{cusp}}/2)}{\pi^2 m^2}} + \frac{\Delta_{\text{ip}}}{V_{\text{p,DC}}}
\]

\[
d_{\text{min}} = d_{\text{HB3}}^{\text{ZVS(cusp)}} - d_{\text{HB4}}^{\text{ZVS(cusp)}} \tag{5.13a}
\]

\[
d_{\text{min}} = \frac{\frac{K\pi}{w_{\text{op}} L[K + 2\chi(1 - \chi)]} \sum_{n=1}^{\infty} \frac{8\sin^2(m\alpha_{\text{cusp}}/2)}{\pi^2 m^2} \sum_{m=1}^{\infty} \frac{8}{\pi^2 m^2}}{\sum_{n=1}^{\infty} \frac{8\sin^2(m\alpha_{\text{cusp}}/2)}{\pi^2 m^2}} - \frac{\Delta_{\text{ip}}}{V_{\text{p,DC}}}
\]

\[
d_{\text{min}} = d_{\text{HB1}}^{\text{ZVS(cusp)}} \tag{5.13b}
\]

Eqn. (5.13) can be rearranged to make the modified coupling co-efficient as the target, i.e.

\[
K|_{\text{min}} = \frac{2(\chi - 1)(\alpha_{\text{cusp}} - 2\rho_{\text{DT}_p}) + \Delta_{\text{ip}} w_{\text{op}} L}{[1 - 2(1 - \chi)] \pi (\alpha_{\text{cusp}} - 2\rho_{\text{DT}_p}) - \Delta_{\text{ip}} w_{\text{op}} L} 2\chi(1 - \chi)] - d_{\text{min}} \pi \tag{5.14a}
\]

\[
K|_{\text{min}} = \frac{d_{\text{min}} \pi 2\chi - \Delta_{\text{ip}} w_{\text{op}} L}{\alpha_{\text{cusp}} + \Delta_{\text{ip}} w_{\text{op}} L} 2\chi(1 - \chi)] - d_{\text{min}} \pi [1 - 2\chi] \tag{5.14b}
\]

Eqn. (5.14) represents two equations with two unknown variables (\( \alpha_{\text{cusp}} \) and \( K \)), and hence can be solved to determine values for these variables for any particular transformer leakage inductance, leakage winding split and DC-DC bus voltage minimum ratio requirements (analytical solution for \( \alpha_{\text{cusp}} \) presented in Appendix B).
5.2. DETERMINING THE REQUIRED REDUCTION IN MAGNETISING INDUCTANCE

Maximum DC-DC Bus Voltage Ratio

A similar process can be used to determine the minimum reduction in magnetising inductance required to maintain continuous ZVS operation at the maximum DC-DC bus voltage ratio condition, under the 3-level modulation conditions of $\alpha = \pi$ and variable $\beta$. Once again, the limiting condition is when the DC-DC bus voltage ratio at the cusp of the primary bridge ZVS boundary is the same as the DC-DC bus voltage ratio at the cusp of the secondary bridge ZVS boundary, and also equals the maximum designed bus voltage ratio $d_{\text{max}}$, i.e.

$$d_{\text{ZVS}_p(\text{cusp})} = d_{\text{ZVS}_s(\text{cusp})} = d_{\text{max}}$$  \hspace{1cm} (5.15)

Under these conditions, $\alpha = \pi$ and $\beta \in [0, \pi] = \beta_{\text{cusp}}$ (now $\alpha$ typically equals $\pi$ for a DC bus voltage ratio of greater than unity). For this case, only the cusp points for HB1/HB2 and HB4 need to be considered for operation in the positive power transfer region ($\delta > 0$), since these phase legs always have the closest two cusp points, and they occur similarly at

$$\delta_p = |\alpha - \beta_{\text{cusp}}|/2 + \rho_{\text{DT}_p} \quad \text{for HB1 and HB2}$$  \hspace{1cm} (5.16a)

$$\delta_n = |\alpha - \beta_{\text{cusp}}|/2 \quad \text{for HB4}$$  \hspace{1cm} (5.16b)

Reflecting from (5.15) into the revised 3.18(a) and 3.18(d) then gives ZVS DC bus voltage ratio boundary limits at these cusp points of

$$d_{\text{max}} = K\pi \frac{w_{\text{sw}} L_{\text{cusp}}(1-K)}{w_{\text{sw}} L_{\text{cusp}}(1-K)} \sum_{n=1}^{\infty} \left[ \frac{\pi}{\sin^2(m \beta_{\text{cusp}}/2)} \left( \frac{8 \pi^2 m^2}{2 \rho_{\text{DT}_p}} \right) + \frac{\Delta i_{\text{p}}}{v_{\text{p,DC}}} \right]$$

$$= d_{\text{HB4/ZVS(\text{cusp})}}$$  \hspace{1cm} (5.17a)

$$d_{\text{max}} = K\pi \frac{w_{\text{sw}} L_{\text{cusp}}(1-K)}{w_{\text{sw}} L_{\text{cusp}}(1-K)} \frac{1 - 2\rho_{\text{DT}_p} \pi}{\pi} \sum_{n=1}^{\infty} \left[ \frac{\pi}{\sin^2(m \beta_{\text{cusp}}/2)} \left( \frac{8 \cos(m \beta_{\text{cusp}}/2)}{\pi^2 m^2} \right) \right] - \frac{\Delta i_{\text{p}}}{v_{\text{p,DC}}}$$

Figure 5.8: Exemplar cusp operating condition at $d_{\text{max}}$ ($\beta = \beta_{\text{cusp}}$)
Figure 5.9: ZVS design requirement of coupling co-efficient for adaptive 3-level PSSW modulation

\[
K^{ZVS} = \frac{\pi + 2\pi(1-\chi)(1-K)}{w_{SW} L_s (K + 2(1-\chi)(1-K))} \left(1 - \frac{2\pi V_{DC}}{\pi}\right) - \frac{\Delta V_{DC}}{V_{DC}} \frac{\beta_{cusp}}{\pi} \\
= d_{ZVS(cusp)}^{HB1} = d_{ZVS(cusp)}^{HB2}
\] (5.17b)

Eqn. (5.17) can be similarly rearranged to make the modified coupling co-efficient \( K \) as the target, viz

\[
K\bigg|_{d_{\text{max}}} = \frac{2\pi(\chi - 1)(1 - \frac{2\pi V_{DC}}{\pi}) + \frac{\Delta V_{DC}}{V_{DC}}[2\chi(1-\chi)]}{1 - 2(1-\chi)]\pi(1 - \frac{2\pi V_{DC}}{\pi}) - \frac{\Delta V_{DC}}{V_{DC}}[1 - 2\chi(1-\chi)] - d_{\text{max}}\beta_{cusp}}
\] (5.18a)

\[
K\bigg|_{d_{\text{max}}} = \frac{d_{\text{max}}\beta_{cusp}2\chi - \frac{\Delta V_{DC}}{V_{DC}}[2\chi(1-\chi)]}{\pi + \frac{\Delta V_{DC}}{V_{DC}}[1 - 2\chi(1-\chi)] - d_{\text{max}}\beta_{cusp}[1 - 2\chi]}
\] (5.18b)

which again can be solved to determine values of \( \beta_{cusp} \) and \( K \) for any particular transformer leakage inductance, leakage winding split and DC-DC bus voltage maximum ratio requirements (analytical solution for \( \beta_{cusp} \) presented in Appendix B).

**Final Selection of \( K \)**

Since (5.14) and (5.18) allow minimum values of \( K \) to be determined for the minimum and maximum required DC-DC bus voltage ratio respectively, the largest possible design value for \( K \) is clearly the smaller of these two solutions, i.e.

\[
K^{ZVS}_{\text{max}} = \min \left\{ K\bigg|_{d_{\text{min}}}, K\bigg|_{d_{\text{max}}} \right\}
\] (5.19)

Fig. 5.9(a) shows the required coupling factor reduction and 3-level modulation duty cycles (primary bridge \( \alpha_{cusp} \) or secondary bridge \( \beta_{cusp} \) as appropriate) as the DC-DC voltage design ratio limits are varied, for a DAB with ideal switches. Note that in contrast to the 2-level solution, \( K = k_T \) is always equal to 1 for the ideal switching case, which can be confirmed by a moment’s reflection recognising that with 3-level modulation, the horizontal ZVS line in Fig. 5.3(a) can always be moved to suit the actual DC-DC bus voltage ratio without requiring any transformer design modification.
5.3. IMPACT OF COUPLING FACTOR ON RMS CURRENTS AND POWER TRANSFER

Fig 5.9(b) shows the matching results for a practical DAB converter where device capacitances and dead-time effects have been included into the analysis, using the operating conditions in Table 6.3 and with transformer parameters of $L = 3.35 \mu H$ and $\chi = 0.67$ as per Table 6.2. Note that a reduced value of $K$ is still required to maintain ZVS across the entire DAB operating range. However, in contrast to the 2-level solution shown in Fig. 5.6(b), this value remains relatively high across a wide range of maximum and minimum DC-DC bus voltage ratios. Hence the increased circulating current required to maintain continuous ZVS under 3-level modulation will be less than the current required to maintain continuous ZVS under 2-level modulation, which will certainly improve the converter’s operating efficiency.

5.3 Impact of Coupling Factor on RMS Currents and Power Transfer

Having determined the minimum required reduction in coupling co-efficient $K$, this section now explores the effects of such a design change on the DAB AC link RMS circulating currents and on its maximum power transfer capability.

Inserting (5.4) into (3.4) the AC link currents can be expressed for each particular harmonic frequency $m$ as

$$I_{p,m}\sin(\theta_{p,m}) = \frac{8dV_p, DC}{m^2\pi\omega m L K + 2x(1-x)(1-K)} \sin(m\delta) \sin\left(\frac{m\pi}{2}\right)$$

$$I_{s,m}\sin(\theta_{s,m}) = -\frac{8dV_s, DC}{m^2\pi\omega m L K + 2x(1-x)(1-K)} \sin(m\delta) \sin\left(\frac{m\pi}{2}\right)$$

(5.20)

noting that for $K \leq 1$ the commonly assumed ideal relationship of $I_{p,m} \angle \theta_{p,m} = -I_{s,m} \angle \theta_{s,m}$ is no longer true because the magnetising current is now non-zero. The overall RMS currents can then be expressed as

$$I_{s,rms}(\delta) = \sqrt{\sum_{n=1}^{N} \left(\frac{I_{n,rms}(\theta)}{2}\right)^2} x \in \{p, s\}$$

(5.21)

Fig. 5.10(a) now shows the relative increase of the RMS AC link currents, defined as

$$\Delta I_{rms} = \frac{\sqrt{I_{p,rms}I_{s,rms} - I_{rms}|K=1}}{I_{rms}|K=1}$$

(5.22)

for a DAB using 2-level modulation as $K$ reduces for different values of the load angle $\delta$, compared to an ideally AC coupled DAB ($K=1$) where $I_{p,rms} = I_{s,rms}$. Note that 2-level operation is the worst-case scenario because the volt-second area applied across the reduced magnetising inductance creates the maximum possible magnetising current for given DC bus voltages. It can be seen from this figure that the relative increase in RMS current reduces substantially as the load angle increases. Since this trend nicely complements the common increase of conduction losses that occurs with high power transfer levels, the increased magnetising current does not significantly impact the VA ratings and the thermal limitations of the converter. Fig. 5.10(a) also shows that a moderate reduction in coupling factor (as can be achieved using 3-level bridge modulation as shown in Section 4.2) only significantly increases the
Figure 5.10: Impact of coupling factor on other relevant DAB performance indicators ($d=1$)

RMS circulating current for small load angles, i.e. for low power conditions.

Finally, the impact of a reduction in transformer coupling factor on the power transfer capability of a DAB is explored. Substituting (5.4) into (5.20) and then into the generic power transfer relationship (7.12), creates a power transfer expression for a DAB with reduced coupling factor, to be

$$P_{0,DC} = P_{s,DC} = \frac{4dV_{p,DC}^2}{w_0L} \cdot \frac{K + 2\chi(1-\chi)(1-K)}{K} \sum_{n=1}^{\infty} \frac{8 \sin(m\delta)}{m^3}$$

$$= \frac{d(2V_{p,DC})^2K}{w_0\pi L[2\chi(1-\chi)(1-K)]} \delta \left(1 - \frac{|\delta|}{\pi}\right) \left|\delta\right| \leq \pi$$

(5.23)

which is dependent on both the modified coupling coefficient $K$ and the leakage inductance split $\chi$.

Fig. 5.10(b) shows how the maximum DAB power transfer capability $P_0$ reduces with $K$ for different values of leakage split, with otherwise identical circuit parameters. In particular, it is interesting to note that this reduction in power transfer gets less as the leakage winding split becomes more asymmetrical ($\chi \to 0$ or $\chi \to 1$), which can be explained by recognising that the imbalance moves the magnetising inductance more towards either the primary or secondary bridge, and so reduces the influence that the magnetising current has on the power transfer process.

### 5.4 Summary

This chapter has extended the commonly used single series impedance model to a more complex AC coupling network with multiple inductance parameters. The investigation has identified that hard switching operating regions always occur for the conventional transformer modeling technique. It has then been shown how a deliberately reduced transformer coupling co-efficient expands the ZVS region at constrained operating points to achieve continuous ZVS operation. An adaptive 3-level modulation concept can be used to maintain the transformer coupling co-efficient as high as possible, which increases the additional RMS circulating currents only as much as is required to benefit from the additional magnetising current and to maintain highest possible conversion efficiency.
6 Practical Validation of ZVS Channel Operation

After identifying the transformer design requirements, several transformer design examples are briefly evaluated by matching Finite Element Analysis (FEA) simulations and impedance measurements. This step is required to show how such a reduced coupling transformer with minimal AC winding resistance can be physically designed. The proposed design approach has then been validated using an experimental DAB prototype, while the airgap of the selected low coupling transformer is adjusted for each PSSW modulation concept to design for an as high as possible magnetising inductance. Finally, it is shown how the proposed design and operation techniques influence the DAB efficiency for a customised DAB prototype.

6.1 Design of a Reduced Coupling Factor HF Transformer

The DAB transformer provides the galvanic isolation between the two bridges and its turns ratio allows to pre-align for a bias voltage boost ratio between the two DC buses. The transformer admittance matrix \([Y]\) immediately translates the bridge output voltage pattern into AC link current waveforms which are then rectified by the bridge switching functions to create the DC bus current (Chapter 7). Hence for a DAB, the coupling high-frequency (HF) transformer is the key component to maximise the efficiency and power density (if no external inductor is added in series). The monotonic circuit model in Fig. 5.1 comprises primary and secondary AC winding resistances \(R_{\sigma,p}\) and \(R'_{\sigma,s}\), primary and secondary coil leakage inductances \(L_{\sigma,p}\) and \(L'_{\sigma,s}\), and a magnetising inductance \(L_m\) (note that the core loss equivalent resistance and intra-winding coupling capacitance are not included in this analysis). All these parameters are referred to the primary side via the physical turns ratio \(N_p/N_s\).

In the previous section, the impedance relationships of a lossless DAB transformer have been determined to maintain continuous ZVS operation throughout the entire operating range. This section now explores how the transformer parameters can be determined using FEA and how they can be tuned by design to achieve a reduced coupling factor transformer with minimal HF resistance.

The transformer coupling factor \(k_T\) in (5.1) and the modified parameter \(K\) in (5.3) can generally

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1 Material in this chapter was first published in:
be influenced in two ways: increasing the total leakage inductance (for a finite magnetsing inductance) and/or reducing the magnetising inductance (for a non-zero leakage inductance). The first approach can practically be achieved by separation of the two windings to increase the average distance between them, the second approach can be implemented by deliberately increasing the core airgap (recognising that a minimum airgap is essential to manage DC flux generation caused by the switching process of both transient and steady-state operation). Similarly, the distribution of leakage flux between the primary and secondary coils is influenced by factors such as the compactness of the winding material (e.g. foil vs. round wire) and by the location of the individual coils in relation to the high permeability magnetic path (i.e. the core).

6.1.1 Finite Element Analysis (FEA)

Unfortunately it can be quite challenging to achieve a precise estimation of the transformer impedance parameters using conventional analysis [54], which typically assumes simplified conductor geometries, average coil-to-coil or coil-to-core dimensions, and does not accommodate frequency dependencies which can cause a significant deviation (particularly as operating frequencies further increase) with respect to the AC winding resistance [68] and the leakage inductances [109].

Hence, a 2D FEA simulation [127] is used in this section to precisely calculate the transformer impedances for a single phase two-winding HF transformer. Note that the design evaluation has been limited to EPCOS ETD59 N87 ferrite cores [128] with an initial material permeability $\mu_r$ of 2200.

Leakage and Magnetising Inductance

From fundamental knowledge, the relationship between flux $\Psi$ and inductance $L$ for a two-winding transformer can be expressed as follows:

$$
\begin{bmatrix}
\Psi_{m,p}^m \\
\Psi_{s,m}^m
\end{bmatrix} =
\begin{bmatrix}
L_{m,p}^m + L_{m}^m & L_{m,m}^m \\
L_{m,m}^m & L_{m,s}^m + L_{m}^m
\end{bmatrix}
\begin{bmatrix}
I_{m,p}^m \\
I_{m,s}^m
\end{bmatrix}
$$

(6.1)

![2D sketch and major design parameters of E/E-core based transformer](image)
The individual transformer inductances can be individually determined from (6.1), viz

\[ L_{m, \sigma, p} = \frac{\psi_m}{I_m^{p=1A, I_m^{s}=0A}} - L_m \]  \hspace{1cm} (6.2a)

\[ L_m = \frac{\psi_s}{I_m^{p=1A, I_m^{s}=0A}} \frac{\psi_p}{I_m^{p=0A, I_m^{s}=1A}} \frac{N_p}{N_s} \]  \hspace{1cm} (6.2b)

\[ L_{m, \sigma, s} = \frac{\psi_m}{I_m^{p=0A, I_m^{s}=1A}} - L_m \]  \hspace{1cm} (6.2c)

Following (6.2) the FEA simulation is parameterised to excite the two windings separately (i.e. \( I_p^m = 1A \) and \( I_s^m = 0A \), or vice versa) using a normalised excitation current at any particular harmonic frequency \( m \). Note that in particular the magnetising inductance \( L_m^m \) can be influenced by non-linear variations of temperature, frequency, flux, etc. to affect the core permeability [128]. Note also that this impact reduces for an increasing core airgap dimension \( l_{gap} \) as is confirmed by the analytical definition:

\[ L_m \approx \frac{A_e}{2l_{gap}} + \frac{N_p^2}{N_s^2} \mu_0 \]  \hspace{1cm} (6.3)

**High-Frequency Winding Resistance**

Again, FEA is used to determine the primary and secondary coil AC resistance values at each particular harmonic frequency \( m \) as they can be immediately derived from the winding loss \( P_{\text{cond}} \) for simultaneous coil current excitation, to become

\[ R_{m, \sigma, p} = \frac{P_{\text{cond}, p}}{1A_{\text{rms}}} \]  \hspace{1cm} (6.4a)

\[ R_{m, \sigma, s} = \frac{P_{\text{cond}, s}}{1A_{\text{rms}}} \left( \frac{N_p}{N_s} \right)^2 \]  \hspace{1cm} (6.4b)

Note that [127] uses a homogenized analytical approximation model to account for the high-frequency dynamics in Litz wire bundles.

**6.1.2 Validation of FEA Simulation**

Due to 2D FEA limitations, the leakage inductance and AC resistance parameters need to be scaled with the ratio between the simulation depth and the actual average coil ellipse contour length (note that this presumes a rotational symmetry of the transformer), while the magnetising inductance requires linear adjustment according to (6.3) if the core cross section area \( A_e \) is circular rather than rectangular.

**Increasing the Winding Separation**

Table 6.1 presents the impedance results based on the FEA simulation and short circuit measurements (using a WayneKerr 6500B device) for the four exemplar transformer designs shown in Fig. 6.2 at
6.1. DESIGN OF A REDUCED COUPLING FACTOR HF TRANSFORMER

multiple (most relevant: \( m = 1, 3, 5 \)) harmonic frequencies of 20 kHz for a minimum 0.2 mm core airgap. Table 6.1 (a) and (b) compare the total series leakage inductance and AC resistance for two transformer designs that illustrate the impact of a winding separation by offset (PROT 2) versus the conventional design approach (PROT 1). As could be expected, the separation of the windings results in a significantly increased total leakage inductance [54] [129] despite the higher turns count for PROT 1. Fig. 6.3 (a) and (b) then show that PROT 2 has a lower DC resistance compared to PROT 1 which can be simply explained by the reduced number of turns (and hence the reduced wire length). However, the resistance of PROT 2 increases faster with frequency causing the two values to become equal at about 90 kHz. Fig. 6.3 (c) and (d) then compare the total leakage inductance and AC resistance for two transformer designs where the gap between the two windings is increased by reducing the secondary winding copper wire diameter from PROT 3 to PROT 4. This design change causes the total leakage inductance and DC resistance of PROT 4 to become larger than the respective values of PROT 3. However, these figures show that the physical arrangement of the conductors causes the resistance to increase less with frequency and hence achieves a lower AC resistance for operating frequencies above 20 kHz.

![Transformer designs using an ETD59 N87 core](image-url)
It can hence be concluded that there are different ways to separate the two windings, which eventually increase the total leakage inductance of the HF transformer and, in turn, reduce the coupling factor for a finite magnetising inductance. On the other hand, the impact on high-frequency AC resistance (i.e. current squeezing) caused by winding separation is not so obvious, since certain physical arrangements (wire diameters, gap between coils, etc.) emphasize the dynamic phenomena (in particular: skin and proximity effect) in different ways.

### Increasing the Core Gap

Eqn. (6.3) indicates that there are rather independent design parameters, namely the core gap dimension $l_{\text{gap}}$, the core material permeability $\mu_r$ and the effective core length $l_e$, that can be selected to adjust the magnetising inductance while (almost) remaining the same amount of total leakage inductance. In Section 6.2, the core gap is adjusted to design for a particular (as high as possible) value of magnetising inductance as has been determined in the previous analysis of Chapter 5. Table 6.2 and Fig. 6.4 show the effect of an increasing core gap on the single impedance parameters and (modified) coupling coefficient for the selected transformer design PROT 4 at an operating frequency of 20 kHz. To adjust the

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PROT 1 ($k_T = 0.994, \chi = 0.48$)

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PROT 2 ($k_T = 0.948, \chi = 0.77$)

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<tr>
<td>$L_{\sigma,p}(\text{FEA})$</td>
<td>1.41</td>
<td>1.40</td>
<td>1.39</td>
</tr>
<tr>
<td>$L_{\sigma,s}(\text{FEA})$</td>
<td>0.42</td>
<td>0.42</td>
<td>0.41</td>
</tr>
<tr>
<td>$L_{\sigma}(\text{FEA})$</td>
<td>1.83</td>
<td>1.82</td>
<td>1.80</td>
</tr>
<tr>
<td>$L_{\sigma}(\text{Meas})$</td>
<td>1.89</td>
<td>1.88</td>
<td>1.85</td>
</tr>
<tr>
<td>$R_{\sigma,p}(\text{FEA})$</td>
<td>1.70</td>
<td>2.00</td>
<td>3.00</td>
</tr>
<tr>
<td>$R_{\sigma,s}(\text{FEA})$</td>
<td>3.90</td>
<td>11.00</td>
<td>30.60</td>
</tr>
<tr>
<td>$R_{\sigma}(\text{FEA})$</td>
<td>5.60</td>
<td>13.00</td>
<td>33.60</td>
</tr>
<tr>
<td>$R_{\sigma}(\text{Meas})$</td>
<td>6.22</td>
<td>15.30</td>
<td>36.90</td>
</tr>
<tr>
<td>$L_m(\text{FEA})$</td>
<td>16.5</td>
<td>16.5</td>
<td>16.5</td>
</tr>
</tbody>
</table>

PROT 4 ($k_T = 0.925, \chi = 0.58$)

Table 6.1: Transformer parameters for varying frequency ($L$ in $\mu$H, $R$ in mΩ @ 25°C)
core gap dimension, multiple layers of isolation material (thickness of each layer: 0.17 mm - 0.2 mm) were stacked in between the two E-shaped cores and fixed by a metal clip at each end of the bobbin. The FEA simulations have been verified with open circuit impedance measurements. Under low coupling conditions, the secondary-side leakage inductance (from FEA) has been subtracted from the measured open-circuit impedance to determine the magnetising inductance $L_m$.

$$K = \frac{2L_m}{L_{(total)} + 2L_m}$$

$$\chi_{(total)} = 0.66$$

Table 6.2: PROT 4 parameters for varying airgap incl. connection impedance ($L$ in $\mu$H, $R$ in m$\Omega$ @ 25°C)

<table>
<thead>
<tr>
<th>$l_{gap}(FEA)$ in mm</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_{m}(FEA)$</td>
<td>16.5</td>
<td>9.01</td>
<td>6.27</td>
<td>4.83</td>
<td>3.95</td>
</tr>
<tr>
<td>$L_{\sigma,p}(FEA)$</td>
<td>1.53</td>
<td>1.55</td>
<td>1.57</td>
<td>1.59</td>
<td>1.60</td>
</tr>
<tr>
<td>$L_{\sigma,s}(FEA)$</td>
<td>1.13</td>
<td>1.10</td>
<td>1.09</td>
<td>1.07</td>
<td>1.05</td>
</tr>
<tr>
<td>$L_{(total)}$</td>
<td>2.23</td>
<td>2.25</td>
<td>2.27</td>
<td>2.29</td>
<td>2.30</td>
</tr>
<tr>
<td>$L_{(total)}$</td>
<td>3.36</td>
<td>3.35</td>
<td>3.36</td>
<td>3.36</td>
<td>3.35</td>
</tr>
<tr>
<td>$K$</td>
<td>0.91</td>
<td>0.84</td>
<td>0.79</td>
<td>0.74</td>
<td>0.70</td>
</tr>
<tr>
<td>$\chi_{(total)}$</td>
<td>0.66</td>
<td>0.67</td>
<td>0.67</td>
<td>0.68</td>
<td>0.68</td>
</tr>
<tr>
<td># layers (Experiment)</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>$L_{m}(Meas)$</td>
<td>17.8</td>
<td>10.2</td>
<td>7.41</td>
<td>5.95</td>
<td>5.08</td>
</tr>
</tbody>
</table>
6.2 Experimental Results

The principles of maintaining ZVS operation as presented in Chapter 5 have been validated using an experimental DAB converter with the specifications listed in Table 6.3. Note that with an ideal converter, i.e. no device capacitance and no phase leg dead-time, ZVS can be maintained across its entire DC bus operating voltage range by simply varying $\alpha$ or $\beta$ to move the (ideal) ZVS channel to match any particular values of DC bus voltages. Under these conditions the transformer coupling factor does not need to change from its ideal value of $K = 1$ (i.e. infinite magnetising inductance), while the 3-level modulation duty cycles are varied to match any particular bus voltage ratio. However, it should be noted that $\alpha_{\text{cusp}}$ at $d_{\text{min}}$ and $\beta_{\text{cusp}}$ at $d_{\text{max}}$ are not balanced in Fig. 5.9 because the transformer turns ratio of $N_p : N_s$ was set higher than a more conventional DC bus voltage centered ratio value of $N_p : N_s = 27V/215V = 1:8.0$ to suit the practical converter, as discussed below.

For the practical experimental converter with device capacitance and phase leg dead-time as listed in Table 6.3, the first step in the transformer design process is to determine whether sufficient leakage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary DC bus voltage $2V_{p,DC}$</td>
<td>24 V - 30 V</td>
</tr>
<tr>
<td>Secondary DC bus voltage $2V_{s,DC}$</td>
<td>200 V - 230 V</td>
</tr>
<tr>
<td>Rated converter power</td>
<td>1 kW</td>
</tr>
<tr>
<td>Switching frequency $f_{sw}$</td>
<td>20 kHz</td>
</tr>
<tr>
<td>Transformer Turns Ratio $N_p : N_s$</td>
<td>1:8.5</td>
</tr>
<tr>
<td>Min. DC-DC voltage ratio $d_{\text{min}}$</td>
<td>0.78</td>
</tr>
<tr>
<td>Max. DC-DC voltage ratio $d_{\text{max}}$</td>
<td>1.13</td>
</tr>
<tr>
<td>IGBT modules</td>
<td>$C_{\text{o}}$ $\approx 288$ pF @ 24V, 1MHz</td>
</tr>
<tr>
<td>4x Infineon BSM75GBN60</td>
<td></td>
</tr>
<tr>
<td>Min. ZVS current (prim. bridge) $\Delta i_p$</td>
<td>5 A</td>
</tr>
<tr>
<td>Min. ZVS current (sec. bridge) $\Delta i_s$ ($\Delta i_s'$)</td>
<td>1.5 A (12.7 A)</td>
</tr>
<tr>
<td>Dead-time angle (prim. bridge) $\rho_{DT_p}$</td>
<td>0.13 rad @ 20 kHz</td>
</tr>
<tr>
<td>Dead-time angle (sec. bridge) $\rho_{DT_s}$</td>
<td>can be neglected</td>
</tr>
</tbody>
</table>

Table 6.3: Experimental system and selected ZVS operating conditions
impedance can be created between the primary and secondary windings to avoid the need for a separate series AC inductor. The target here is to have enough series impedance so that at the maximum power displacement angle $\delta_m$, the converter operates beyond the two cusp inflection points shown in Fig. 5.3(f). The coupling transformer arrangement that was developed to achieve this is shown in Fig. 6.2(d), with the two windings located as far away from each other as possible on the core centre limb. This achieved a total transformer series leakage inductance of 2.66 $\mu$H, as predicted by the Finite Element Analysis (FEA) procedure that was used to design the transformer and then confirmed by direct measurement, as shown in Table II. With this inductance, the maximum power displacement angle is $\delta_m \approx 0.7$ rad $= 40^\circ$, which is well beyond the cusp points. Hence an additional series inductance is not required.

To decrease the transformer coupling factor (i.e. in this context: increase the magnetising current) the core airgap shown in Fig. 6.1 was increased in 0.2 mm steps up to 1.0mm, as has already been discussed. Table 6.2 shows the results of this change, determined by FEA analysis with confirming experimental measurements shown in Fig. 6.4 for the magnetising inductance. (Note that the experimental measured points for $L_m$ were taken at slightly different airgap steps, because the material used to gap the core had a thickness of slightly less than 0.2mm per strip.) The estimated additional 700 nH introduced by the external (primary) transformer connections was then added to the primary leakage inductance calculated by FEA analysis, and the values of $K$ and $\chi$ shown in the last rows of Table 6.2 were calculated using these results. The converter primary and secondary bridge phase legs were constructed using IGBTs (relevant primary-side IGBT module resistance of $2 \times 10^{-3}$ m$\Omega$ was included in the analytical model), while the DC buses were created using standard DC power supplies with parallel load banks to allow energy to be received as required. A switching frequency of 20 kHz was used, with a significant primary bridge dead-time period of 1.0 $\mu$s (equals 0.13 rad at 20 kHz) to account for reduced speed gate driver actuation to limit the device voltage overshoot obtained when switching high magnitude currents at low DC bus voltage levels, and a negligible secondary bridge dead-time. The minimum ZVS currents shown in Table 6.3 were set a little higher than was actually required to match the IGBT device parasitic capacitances, to accommodate variability in these parameter values and parasitic transformer capacitances. ZVS converter operation was verified experimentally under both minimum and maximum DC bus voltage ratio conditions, by setting modulation parameters manually using the controlling DSP to maintain ZVS as the transferred power was varied. The results confirm the ability of the theoretical analysis to design a continuous ZVS channel using a reduced coupling transformer for a practical converter, and then to steer the converter operation through this channel by varying the 3-level duty cycles as the power transfer level changes.

Note that all experimental waveforms presented are referred to the primary AC terminals of the transformer. The converter modulation parameters were set manually using the controlling DSP to achieve the exact operating conditions required for each experimental test.

Section 5.2 has quantified the maximum ZVS (modified) coupling factor $K_{ZVS \max}$ for the conditions listed in Table 6.3 based on a lossless DAB and a 2-level or 3-level modulation concept. For this
CHAPTER 6. PRACTICAL VALIDATION OF CONTINUOUS ZVS OPERATION

experimental work, the airgap of the transformer prototype was modified (Table 6.2) for each modulation concept to adjust the magnetising impedance (and hence the winding coupling factor) to achieve a close match with the predicted values of $K_{ZVS}^{\text{max}}$. Finally, it is commented that the AC link resistance (neglected in Sections 5.2 and 5.3) tends to shift the ZVS regions towards lower DC-DC bus voltage ratios for positive values of $\delta$, and vice versa, as described in Chapter 3.

6.2.1 2-Level Modulation

For 2-level modulation ($\alpha = \beta = \pi$), the analysis of Section 5.2 identifies $K_{ZVS}^{\text{max}}$ as 0.68. From Fig. 6.4, this corresponds to a physical airgap slightly higher than 1.0 mm. Fig. 6.5 shows the ZVS regions for a 1.0 mm airgap, which predicts that the DAB converter can operate under ZVS conditions over (almost) the entire DC bus voltage range that is required.

Fig. 6.6 then plots the primary and secondary coil as well as the magnetising RMS current for both the minimum and maximum DC-DC bus voltage ratios. The total conduction winding loss can be calculated as follows:

$$P_{\text{cond}} = \frac{1}{2} \sum_{n=1}^{N=20} R_{\sigma_p}^m \cdot (I_{mp}^m)^2 + R_{\sigma_s}^m \cdot (I_{ms}^m)^2$$

(6.5)

where $R_{\sigma,x}^m$ is the AC link resistance for each coil respectively for each particular harmonic frequency, and $I_{x}^m$ is the peak value of each harmonic current component calculated using (3.4). The significant increase of magnetising current caused by the large transformer airgap can be seen.

Fig. 6.7 shows selected experimental switching waveforms at the minimum DC-DC voltage ratio of $d = 0.78$ for a power transfer of 100 W (close to cusp operating point). As predicted in Section 5.2 and confirmed by this waveform, the converter is comfortably operating in ZVS for these conditions. Fig. 6.8 shows a matching experimental waveform at the maximum DC-DC voltage ratio of $d = 1.13$ for a transferred power of 250 W (slightly beyond cusp operating point), where the expected slight ZVS violation can be confirmed as the primary phase leg current changes polarity at the end of the primary bridge dead-time period (indicated as thin shadow area) which causes a partial hard switching transition of the primary bridge as indicated and described earlier in Chapter 3.

Figure 6.5: 2-level/2-level ZVS regions @ 1.0 mm airgap
6.2. EXPERIMENTAL RESULTS

6.2.2 Adaptive 3-Level Modulation of One Bridge

Forward Operation

From Section 5.2, the value of $K_{\text{ZVS}}^\text{max}$ required to maintain continuous ZVS using 3-level modulation is slightly below 0.85. According to Fig. 6.4, this corresponds to an airgap dimension of about 0.4 mm.

The additional control degree of freedom obtained for 3-level modulation creates a two-dimensional solution space (when operating away from the ZVS cusp operating points) that still satisfies the power transfer requirement and ZVS boundary condition. Hence, the final modulation parameters are selected such that the total conduction loss in (6.5) are minimised while maintaining ZVS operation.

Minimum DC bus voltage ratio ($\alpha$ variable, $\beta = \pi$)  Fig. 6.9 shows how the narrower ZVS channel (Note: the channel concept has been previously defined in Chapter 5), created by this higher 3-level modulation coupling factor, can be moved by varying $\alpha$ to maintain continuous ZVS operation as the transferred power levels (and thus $\delta$) increases. At low power transfer levels, before the ZVS channel “pinches”, $\alpha$ is set to 2.39, to make the channel straddle the minimum DC bus voltage ratio of $d = 0.78$. This both maintains ZVS and achieves the lowest possible conduction losses for power transfer levels of up to 350 W, as shown in Fig. 6.9(a). Around the cusp operating point, the ZVS channel is moved up by setting $\alpha = 2.77$ to maintain ZVS as the power transfer level increases from 400 W (close
to the cusp operating point) to over 500 W, as shown in Fig. 6.9(b). This compares very well with the
cusp point value of $\alpha = 0.84\pi = 2.64$, as shown in Fig. 5.9(b) using the lossless analysis. Beyond the
cusp operating point, the ZVS channel opens up, and 2-level modulation is restored by setting $\alpha = \pi$
in Fig. 6.9(c), to again achieve the lowest possible RMS currents. Note that the physical turns ratio of
1:8.5 has been selected such that the centre point of the operating range of $d$ is vertically aligned with
the centre point of the ZVS channel for 2-level bridge modulation and an airgap of 0.4 mm.

Fig. 6.10 shows the magnitude of the (required) magnetising and primary/secondary coil currents and
the consequential $I^2R$ winding copper loss for these operating conditions, where the reduced magnetising
current magnitude compared to the previous 2-level modulation concept can be seen. This reduces the
winding losses by 63% at low load condition of 100 W and 28% at the higher load condition of 700 W.
Fig. 6.11 shows experimental waveforms across the three stages, where ZVS has been achieved for all
operating points since the primary and secondary referred bridge current magnitudes at the point of

Figure 6.9: 3-level/2-level ZVS regions @ 0.4 mm airgap

Figure 6.10: 3-level/2-level PSSW modulation @ 0.4 mm airgap ($d = 0.78$)
6.2. EXPERIMENTAL RESULTS

Figure 6.11: Experimental waveforms @ 0.4 mm airgap \( (d = 0.78) \)

switching are outside the \( \Delta i_p \) and \( \Delta i'_p \) limits (shown at the left hand side of these plots). Fig. 6.11(b) for instance also shows the rapid change in \( i_p \) that occurs during the HB1 positive transition dead-time period (shown in grey), which emphasises the importance of ensuring that \( i_p \) stays outside \( \Delta i'_p \) for the entire dead-time period to guarantee ZVS.

Maximum DC bus voltage ratio \( (\alpha = \pi, \beta \text{ variable}) \)  Fig. 6.12 shows the ZVS channel region created by reducing \( \beta \) for this higher DC bus voltage ratio region. In this particular context of coupling impedance and DC-DC bus voltage operating region, only one value of \( \beta = 2.39 \) (compared to \( \beta_{\text{cusp}} = 0.83\pi = 2.61 \) in the lossless model as shown in Fig. 5.9(b)) is sufficient to achieve ZVS and the minimum RMS objective as the power (and thus \( \delta \)) increases. Fig. 6.13 shows the magnitude of the magnetising and primary/secondary currents and the consequential \( I^2R \) winding losses for these operating conditions.

Fig. 6.14 shows the experimental switching waveforms at the 300 W and 400 W power transfer levels (straddling the HB4 cusp), where it can be seen that \( i_s \) is only just outside the \( \Delta i'_s \) limit at the HB4 transition point. This confirms that the converter is only just operating in ZVS at this power transfer level as predicted from Fig. 6.12.

For all results presented above, the analytical model well predicts the converter ZVS conditions
despite further unconsidered second-order effects such as DC bus voltage ripple, device voltage overshoot, device voltage drop and the (non-linear) variation of the effective ferrite core material permeability.

Reverse Operation

Additional experimental results are provided to also confirm continuous ZVS operation in the reverse (i.e. from secondary-to-primary) power flow direction. Fig. 6.15 and 6.17 show the most constrained operating points for \( d = 0.78 \) and \( d = 1.13 \). Fig. 6.16 and 6.18 then present the experimental waveforms for the respective operating points, to confirm the analytical predictions.

6.2.3 Combined 3-Level Modulation

For AC coupled DC-DC converters, the transformer core loss often becomes dominant at low load conditions. However, the DAB topology allows the core magnetising current to be actively decreased in those low power operating regions located away from the most constrained ZVS cusp points towards \( \delta = 0 \), by varying both bridge duty cycles \( \alpha \) and \( \beta \) simultaneously, and thus reducing both bridge volt-second outputs. This provides a lower magnetising current operating point for the low power transfer regions which shrinks the available ZVS regions as shown in Fig. 6.19(a) and Fig. 6.19(b). Hence, as identified in Fig. 6.19, a very precise \( \alpha/\beta \) ratio is required to maintain ZVS converter operation during this power transfer range and \( \beta \) must be set back to \( \pi \) as the power transfer level increases and
the converter moves through the most constrained ZVS region. Fig. 6.20 and 6.21 show a combined 3-level/3-level modulation concept for the minimum and maximum DC bus voltage ratio where $\beta$ and $\alpha$ respectively become $\pi$ again at the cusp operating points. Note that the reduced core magnetisation current implicitly reduces the winding losses (which are however rather low in this region anyway).
6.3 Efficiency Evaluation

As part of a confidential industry project, a customised DAB power stage (rated power: 1.2 kW) has been assembled using the presented design and operation guidelines to maintain continuous ZVS operation by transformer design and adaptive 3-level modulation. It basically replaces the IGBT devices with the latest generation of low voltage MOSFET devices for the primary bridge and adequately sized super-
junction FETs for the HV secondary bridge. The transformer windings were slightly adjusted to account for an increased switching frequency.

A power analyser (ZIMMER LMG 500) was used to measure the converter efficiency. The results presented in Fig. 6.22 show high efficiency values between 96.5% and 98.5% across (almost) the entire operating range. Both power and DC bus voltage values (primary/secondary) are scaled on a per unit basis with respect to their nominal ratings. The auxiliary power supply loss of 0.002 p.u. is not included in the efficiency measurements. The two marked efficiency points in Fig. 6.22 indicate an incomplete ZVS transition, i.e. the circulating phase leg current at the switching transition of the secondary bridge was not sufficient at these (cusp) operating conditions to fully dis-/charge the device charge of the super-junction FETs within the dead-time period. This means that $\Delta i_s$ was selected as slightly too low for this particular design context. Note that the use of wide bandgap semiconductor devices with reduced device charge widens the effective ZVS region, since $\Delta i_s$ can be reduced.

Fig. 6.23 presents the segregated power loss components of the DAB across the entire power range, for three exemplar DC-DC bus voltage ratios. In addition to the copper winding loss (6.5), the developed (temperature-dependent) power loss model also considers the switch device voltage drop characteristic and wide range turn-off loss measurements of the LV and HV switch devices, and a finite element analytical core loss estimation based on the IGSE (Improved Generalised Steinmetz Equation) briefly described in Appendix C. The individual component waveforms were generated using a PLECS [130] circuit simulation.

As could be expected at low power levels, a small percentage increase of $P^2R$ winding losses and switch conduction losses can be observed at partial load conditions. However, since the additional magnetising current is relatively constant over power, they become less significant at higher power levels. Overall,
Figure 6.23: Efficiency measurements and loss breakdown for 3-level/3-level PSSW modulation @ 0.4 mm airgap

both the model and the experiment indicate that the total converter efficiency only slightly reduces over its entire power range, particularly as the DC bus voltages move away from a unity ratio.

The verified power loss model is now further used to illustrate the expected DAB efficiency and loss breakdown for a 2-level/3-level modulated ZVS soft switched DAB with 0.4 mm transformer airgap for \( d = 1.04 \) in Fig. 6.24(a). As could be expected, mainly the core loss is significantly increased at partial load in comparison to Fig. 6.23(a). Fig. 6.24(b) then shows the model results for a 2-level/2-level modulated ZVS soft switched DAB with a 1.0 mm airgap transformer. Due to the heavily reduced magnetising inductance, the conduction loss in the switch devices and the transformer coils increase significantly. The core loss remains similar to Fig. 6.24(a) since the core flux density \( B \) depends on the absolute volt-second output applied from each bridge (defined by the DC bus voltage magnitudes, \( \alpha \))
and $\beta$, the operating frequency $\omega_{sw}$, the number of turns $N$ and the core cross section area $A_e$ and is essentially independent of the core gap dimension itself.

It is commented that the final converter hardware specifications cannot be disclosed in this thesis because of company IP protection issues. Instead, the presented per unit figures are used to confirm the benefits of the proposed design and modulation concepts for any particular DAB application context.

6.4 Constrained ZVS Operation for Off-Nominal Turns Ratio

Irrespective of the analysis strategy and framework used, the ZVS objective that has been conventionally used is to firstly ensure ZVS is achieved over as wide an operating range as possible, and then to adjust the modulation strategy (and sometimes the magnetic component design) to reduce the RMS magnitude of the AC circulating current within this primary ZVS constraint [38] [36] [40] [56]. Unfortunately with this objective, the magnitude of the circulating current at the instant of phase leg commutation can be quite high, particularly for a bridge operating with a low DC bus voltage and a high magnitude output current. If, for instance, the converter boost ratio $d$ is further increased (absolute $d > 10$ without consideration of transformer turns ratio) by reducing the lower voltage (LV) bus voltage while maintaining the same peak power transfer, the LV switching energies will further increase. Consequently even under ZVS conditions, the parasitic loop inductance within the bridge commutation cell can still lead to substantial turn-off switching losses [131], which may become dominant in the overall loss breakdown for such a DAB application and impact the thermal constraints of the LV bridge towards a lower maximum power level.

This section now proposes a constrained ZVS operating strategy to reduce these losses, by ensuring that just sufficient circulating current is flowing into the phase leg at the instant of its bus-to-bus volt-
age transition to guarantee that complete ZVS switching occurs. The approach uses the results of the previous chapters to precisely identify the magnitude of the circulating current at this instant, taking into account second-order effects such as complex link impedance networks, dead-time and device capacitance. It then employs adaptive 3-level bridge output voltage modulation to identify the region where the magnitude of the switched phase leg commutation current is just above the minimum required value to guarantee a complete ZVS charge transition, while also being kept below a maximum switched current magnitude to limit the device losses caused by parasitic inductance. To achieve an adequately wide range for this constrained ZVS operation, careful design of the coupling transformer with a deliberate off-nominal turns ratio and a reduced winding coupling factor is required. The analytical predictions of the proposed strategy have been experimentally verified for a reference DAB system.

6.4.1 Limitation of Maximum Switched Phase Leg Current

Determining the ZVS Transition Current Magnitude

The current magnitudes during each phase leg commutation process can be found by evaluating their solution at various points in time from the device turn-OFF until the active turn-ON of the incoming opposite device (i.e. during the entire dead-time period). Using this approach, the absolute magnitude of each half-bridge current at the associated phase leg switching instant is given by

\[
\begin{align*}
\dot{r}_{\text{H1}} &= \frac{4 V_{\text{p,DC}}}{\pi} \left\{ \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( \gamma_{p,n}^{m} \right) \cos \left( m\alpha \right) \left\{ \cos \left( \gamma_{p,n}^{m} \right) \sin \left( m\delta + \frac{\alpha}{2} \right) \right\} \right. \\
& \quad \left. - 2d \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( m\delta + \frac{\alpha}{2} \right) \right\} \\
\dot{r}_{\text{H2}} &= \frac{-4 V_{\text{p,DC}}}{\pi} \left\{ \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( \gamma_{p,n}^{m} \right) \cos \left( m\alpha \right) \left\{ - \cos \left( \gamma_{p,n}^{m} \right) \sin \left( m\delta + \frac{\alpha}{2} \right) \right\} \right. \\
& \quad \left. - 2d \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( m\delta + \frac{\alpha}{2} \right) \right\} \\
\dot{r}_{\text{H3}} &= \frac{-4 V_{\text{p,DC}}}{\pi} \left\{ -d \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( \gamma_{p,n}^{m} \right) \cos \left( m\beta \right) \left\{ - \cos \left( \gamma_{p,n}^{m} \right) \sin \left( m\delta + \frac{\beta}{2} \right) \right\} \right. \\
& \quad \left. + 2 \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( m\alpha \right) \right\} \\
\dot{r}_{\text{H4}} &= \frac{-4 V_{\text{p,DC}}}{\pi} \left\{ -d \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \cos \left( \gamma_{p,n}^{m} \right) \sin \left( m\beta \right) \left\{ \cos \left( \gamma_{p,n}^{m} \right) \cos \left( m\delta + \frac{\beta}{2} \right) \right\} \right. \\
& \quad \left. + 2 \sum_{n=1}^{\infty} \frac{Y_{p,n}^{m}}{m} \sin \left( m\alpha \right) \right\} \\
\end{align*}
\]
where \( i_{\text{HB}i} \) \((i \in \{1, 2, 3, 4\})\) is positive if the phase leg output current of HB\(i\) flows into the phase leg as the lower device turns OFF (ZVS condition).

### 6.4. CONSTRAINED ZVS OPERATION FOR OFF-NOMINAL TURNS RATIO

**Constraining the ZVS Region to Minimise the Switched Phase Leg Current**

To achieve reliable ZVS transition, the ingoing phase leg current needs to be evaluated during the entire dead band period, i.e. for \( r = 0 \) and \( r = 1 \) (and all values in between), to determine the minimum (absolute) current magnitude required during this period. Note that depending on the derivative of the load current (i.e. the operating condition) the dead-time correction may or may not influence the actual ZVS boundaries, as emphasized in Chapter 3. The ZVS conditions can be re-written as follows:

\[
\min_r \{ i_{\text{HB}1}, i_{\text{HB}2} \} \geq \Delta i_p \quad \text{(HB1 and HB2) (6.7a)}
\]

\[
\min_r \{ i_{\text{HB}3}, i_{\text{HB}4} \} \geq \Delta i_s \quad \text{(HB3 and HB4) (6.7b)}
\]

where \( \Delta i_p \) and \( \Delta i_s \) are (again) the minimum absolute phase leg current magnitudes that must be maintained during a dead-time period, to inject sufficient charge into the phase leg device capacitances to reliably achieve a ZVS bus-to-bus voltage transition, as is illustrated in Fig. 3.12.

For a lower voltage (LV) primary bridge DC bus, the switch power loss \( P_{\text{sw,loss}} \) can be determined from [131] using an analytical switch loss model of high-current MOSFET devices (typically the most suitable for these applications) to be

\[
P_{\text{sw,loss}} = \frac{L_{\text{par}} V_{\text{BR,DSS}} (i_{\text{HB}1/2})^2}{2(V_{\text{BR,DSS}} - 2V_{\text{p,DC}}) f_{\text{sw}}} \quad (6.8)
\]

where \( L_{\text{par}} \) is the total parasitic commutation loop inductance and \( V_{\text{BR,DSS}} \) is the rated device breakdown voltage. Since the lower boundary of \( L_{\text{par}} \) is usually practically limited by the physical constraints of the component dimensions, (6.8) identifies that the switching loss can only be effectively reduced by lowering the initial turn-off current magnitude \( i_{\text{HB}1/2} \) (for a target switching frequency \( f_{\text{sw}} \)).

If \( r = 0 \) is selected in (6.6) no dead-time correction is included into the analysis and the phase leg current is solely evaluated at the point of device turn-OFF. This evaluation can now be used to determine the initial amount of switched commuation current. The additional constraint to limit the ZVS turn-OFF current magnitude to values below the maximum accepted value of \( i_{\text{p,sw}} \) becomes

\[
\begin{align*}
\frac{i_{\text{HB}1}}{i_{\text{HB}2}} & \leq i_{\text{p,sw}} \quad \text{(HB1)} \\
\frac{i_{\text{HB}1}}{i_{\text{HB}2}} & \leq i_{\text{p,sw}} \quad \text{(HB2) (6.9)}
\end{align*}
\]

Using the boundary conditions defined by (6.7) and (6.9), \( \beta \) is now varied to locate a constrained ZVS region, within which a complete ZVS transition will occur while the initial turn-OFF current value is below a maximum value, to match the actual DC bus voltage ratio and power transfer. Fig. 6.25 shows this process. In this figure, the solid blue curve defines the ZVS boundaries for the primary bridge phase legs HB1 and HB2, while the red curve defines the matching ZVS boundaries for the secondary bridge phase legs HB3 and HB4 to guarantee the minimum ZVS turn-OFF current magnitudes \( \Delta i_p \) and
CHAPTER 6. PRACTICAL VALIDATION OF CONTINUOUS ZVS OPERATION

\[ \Delta i_s \]. The dotted blue curve then defines the added primary bridge switched current operating limit for \( d \) as \( \delta \) varies. Below this line the circulating current magnitude at the turn-OFF switching instances will be unacceptably high.

Modulation Strategy and Design Implication

Without loss of generality, the primary bridge is now assumed to be connected to the LV DC bus. This means that it has the higher magnitude circulating current, which must be reduced to as small a value as possible for each bridge phase leg (HB1 and HB2) at their switching instances, to limit their switching losses caused by parasitic loop inductance. This is typically best achieved by ensuring that the two phase leg currents have the same magnitude at their commutation instances, which means that the primary bridge must operate with 2-level PSSW modulation, i.e. \( \alpha \) has to be set to \( \pi \) (radians). Consequently only the secondary bridge duty cycle variable \( \beta \) remains as a degree of freedom to keep the converter operating in the constrained ZVS loss region.

Chapter 5 has identified that 3-level DAB modulation, in conjunction with a lowered coupling factor transformer design, can create a ZVS region that extends across the required operating range of \( \delta \), but only for a limited range of DC bus voltage ratios \( d \). For the condition now where \( \alpha = \pi \), the referred DC-DC bus ratio \( d \) must typically be greater than 1.0, which creates the ZVS regions shown in light grey in Fig. 6.25, according to (6.7). These conditions mean that an off-nominal turns ratio transformer must be used to match these higher values of \( d \) to the actual DC bus voltage windows of the two bridges. The constrained ZVS region is then defined by merging the previous definition (solid line) with the additional constraint (6.9) such that the primary bridge phase leg turn-off currents are below a certain maximum (dotted line), to result in the dark grey area ZVS*.

As already explored in Chapter 3 the center of the ZVS region can be vertically adjusted with the DC-DC bus voltage ratio \( d \) by changing the \( \alpha/\beta \) ratio. It can be seen from the figure that the constrained ZVS* region moves up accordingly towards higher values of \( d \) as the secondary bridge duty cycle \( \beta \) reduces (from 2.8 to 2.0 radians) for a constant primary bridge duty cycle \( \alpha \). In addition, the horizontal width of the “flat section area” increases as the two secondary bridge ZVS boundaries for HB3

![Figure 6.25: Constrained ZVS regions for varying \( \beta \)](image-url)
and HB4 are further misaligned. However, since dead-time effects have been included into this analysis, the constrained ZVS region disappears for larger (positive) values of $\delta$, i.e. where the conditions of a minimum ZVS current magnitude and a maximum initial turn-OFF current conflict.

The maximum forward power transfer limit where the converter is still capable to operate under these ZVS conditions is identified by the intersection of the solid and dotted blue lines. Furthermore, while this power limit can be increased by reducing $\beta$ (from 2.8 to 2.0 radians), this is at the expense of requiring a higher DC bus voltage ratio $d$, which limits the DAB operating context in other ways and inevitably increases the circulating RMS currents in the DAB AC link, as has already been described in [1]. Also, as shown by Fig. 6.25, the secondary bridge phase legs HB3 and HB4 are operated further away from their respective ZVS boundaries inside the constrained ZVS operating region. The proposed design and operating strategy hence forces the secondary converter bridge, connected to the higher voltage DC bus, to always switch the (increased) peak current magnitude of the AC link current (HB3 for $\delta \geq 0$ and HB4 for $\delta \leq 0$). However, as the current magnitudes are generally lower at the high voltage bridge, their switching energy is generally not as critical since a significant step-up transformer turns ratio is assumed to account for an even larger DC-DC bus voltage ratio. Trading off between these competing influences of increased circulating reactive RMS currents versus reduced low-voltage side switching energies now becomes a design/operation optimisation challenge for any particular application context.

### 6.4.2 Experimental Results for Off-Nominal Turns Ratio

An exemplar DAB system is presented to showcase the use of the analysis principles outlined above to achieve a constrained ZVS turn-OFF condition for a DAB with a varying secondary side DC bus voltage, and primary-to-secondary power transfer. Table 6.4 lists the fundamental operating parameters and constrained ZVS conditions for this test system. In order to maintain operation inside the constrained ZVS region, the referred DC-DC ratio is always operated well above $d = 1$ as has been discussed previously. The transformer design of the previous sections (PROT 4) is re-used and has already been characterised in Table 6.2 and 6.3. Note that the turns ratio now becomes significantly off-nominal due to the modified DC-DC voltage ratio operating conditions.

Using (6.6)–(6.9) the PSSW angles $\beta$ and $\delta$ can be determined for a positive power transfer from 100 W to 600 W, to maintain the DAB within the constrained ZVS* region, while the RMS circulating currents in (3.4) were reduced as much as possible in the remaining solution space. Fig. 6.26 shows the analytical predictions for an increasing primary-to-secondary power transfer with $d = 1.47$, as $\beta$ increases from 1.73 to 2.05 radians. For a power transfer of 100 W, $\beta$ is set to be 1.88 radians in Fig. 6.26(b) as a lower value would otherwise violate the boundary condition of (6.7) in Fig. 6.26(a). As the

<table>
<thead>
<tr>
<th>$2V_{p,DC}$</th>
<th>$2V_{s,DC}$</th>
<th>$\Delta i_p$</th>
<th>$\Delta i_s$</th>
<th>$i_{p,sw}^{\text{max}}$</th>
<th>$P_{p,DC}^{\text{max}}$</th>
<th>$d_{\text{min}} / d_{\text{max}}$</th>
<th>$f_{sw}$</th>
<th>$\rho_{DT_p}$</th>
<th>$\rho_{DT_s}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 V</td>
<td>225V - 250V</td>
<td>2 A</td>
<td>1.5 A</td>
<td>20 A</td>
<td>600 W</td>
<td>1.35 / 1.47</td>
<td>20 kHz</td>
<td>0.13 rad</td>
<td>negl.</td>
</tr>
</tbody>
</table>

Table 6.4: DAB prototype and constrained ZVS operating conditions
power (and $\delta$) increases to 200 W and 300 W, $\beta$ reduces to achieve reduced circulating RMS currents in the AC link, and then increases again for 400 W and beyond. At 600 W, the maximum power transfer is reached, as a further increase of $\beta$ or $\delta$ would violate the primary bridge conditions of (6.7) and/or (6.9).

Fig. 6.27 now shows the matching experimental waveforms with marked primary bridge turn-OFF current magnitudes and the dead band periods. Note that the secondary AC link current is intentionally cropped at higher power transfer to maintain visual focus on the primary bridge current waveform at the low voltage DC bus. As can be seen, the DAB converter operates (almost) entirely inside the constrained ZVS region, which shows the validity of the suggested approach. However, as predicted by the analytical model in Fig. 6.27(c), the DAB operates very close to the primary bridge ZVS boundary, which is
6.4. CONSTRANDED ZVS OPERATION FOR OFF-NOMINAL TURNS RATIO

Figure 6.28: ZVS trajectory for reference DAB system ($d = 1.35$)

Figure 6.29: Experimental waveforms for high-boost DAB ($d = 1.35$)

experimentally confirmed by the two bottom plots of Fig. 6.27. The primary bridge output voltage begins to reduce to zero towards the end of the dead-band as the phase leg current changes polarity and the current commutes to the opposing diode, which causes a partial hard switching transition (indicated by the arrows). Note however that for this partial hard switching transition, the opposite diode is still prevented from conducting current as the device capacitors do not become entirely reverse charged. Note that this observation indicates a slight mismatch between the experimental result and the model prediction, mainly traced back to the deviation between the FEA simulation and slightly higher experimentally realised value of magnetising inductance as per Table 6.2 (the subsequent primary bridge ZVS boundary has been re-drawn as solid black line into Fig. 6.26(c)). Further misalignments may occur due to the non-ideal voltage switching pattern (e.g. IGBT voltage drop, finite $dv/dt$ slope transition, DC
bus resistance) and non-linear variations of the AC link impedance network. Of course a safety margin can always be included by increasing the value of $\Delta i_p$. However for this example, the value has been selected very close to the zero current crossing.

An equivalent analysis including experimental validation has been conducted for the minimum DC-DC bus voltage ratio $d = 1.35$. Fig. 6.28 shows the analytical predictions. As the converter is now operating closer to $d = 1$, the values of $\beta$ are generally selected higher to reduce the $\alpha/\beta$ ratio (as compared to $d = 1.47$). Otherwise, it can be observed again that $\beta$ increases with power from 2.04 to 2.70 (note that $\beta$ equals 1.77 at 200 W). Fig. 6.28(c) then shows how a further increase of $\delta$ would not comply with (6.9) any further, which limits the maximum DAB power transfer capability. Fig. 6.29 now shows the matching experimental waveforms, while Fig. 6.30 provides an expanded view of the primary bridge voltage transition at 400 W and 500 W. From the primary bridge current waveform of $i_p$ in these figures it can clearly be seen how the constrained ZVS region (ZVS*) of the primary bridge starts to restrict the marked operating points in Fig. 6.30(b) as $\delta$ (and thus power) increases: while for 400 W, the switched current magnitude $i_{\text{r0}}^\text{HB1/2}$ is still well below $i_p^\text{max}_{\text{sw}}$, it gets closer to this limit at 500 W. On the other hand, both operating points indicate that $i_p$ is just about to change polarity when the ingoing device is gated ON.

### 6.5 Summary

This chapter applied the design guidelines from Chapter 5 to an experimental DAB system to confirm the validity of continuous ZVS operation, and then to a customised DAB prototype to show the impact on the DAB efficiency and power loss distribution. A moderately reduced magnetising inductance in combination with an adaptive 3-level modulation scheme is shown to always maintain ZVS of all four DAB phase legs while the conduction losses are only slightly affected. An alternative DAB design approach has then been presented by introducing a constrained ZVS region to reduce the ZVS device turn-OFF commutation loss for a high-boost DAB, caused by the parasitic commutation inductance.
7 Determination of DC Bus Harmonics

Chapters 3-6 have explored advanced ZVS boundary conditions taking advantage of the proposed Frequency Domain Analysis (FDA) approach. Indeed most research investigations into the DAB topology have focused on design and operating techniques with respect to the AC link. Chapter 7 now applies FDA to investigate the DC bus waveforms, recognising that the Phase Shifted Square Wave (PSSW) modulation process of a DAB injects high-magnitude current harmonics into each DC port at multiples of the primary switching frequency. These harmonics can potentially excite resonances in the $LC$ circuits created by parasitic second-order filter impedances such as wiring inductances in the DC bus connections. The outcome can be substantial voltage and/or current oscillations on the DC buses, particularly when higher switching frequency, wider band-gap devices such as Silicon-Carbide (SiC) or Gallium-Nitride (GaN) devices are used.

This chapter now analytically derives the magnitude and frequency of the DC bus harmonic current components for single phase and three-phase DAB converters, for any DC-DC bus voltage ratio, PSSW modulation parameters and AC link coupling impedances. This analysis is then extended to express the DAB power transfer for any design and operation context.

7.1 Single Phase DAB

Fig. 7.1 shows the topology of a single phase DAB, where the two bridges are (again) coupled by a generic admittance matrix $[Y]$. The typical DC bus arrangement for this topology has high-frequency DC bus capacitors with a finite capacitance $C_{DC}$ and ESR resistance $R_{ESR}$ that are located in close proximity to the bridge semiconductor devices, e.g. ceramic capacitors or film polypropylene (PP) capacitors, to buffer the energy required to support the switching transitions and minimise the stray commutation inductance. A certain distance away, the primary energy source, e.g. electrolyte bulk capacitors or a storage battery, connects to the inner DC bus via a (short) conductor and/or an external discrete choke. This creates a parasitic impedance $L_{DC}/R_{DC}$ that forms a resonant circuit with the inner DC bus capacitance $C_{DC}$, as shown in the figure.

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1Material in this chapter was first published in:
7.1. SINGLE PHASE DAB

### 7.1.1 Fundamentals

The DC bus harmonic current components for any arbitrary operating condition and DAB AC coupling impedance will now be determined using harmonic decomposition analysis of the PSSW switching pattern. In addition, this analysis is used to show how the PSSW modulation parameters and transformer impedance elements influence the DAB power transfer.

Without loss of generality, the analysis is carried out at the primary DAB converter bridge and DC bus. In general terms, the DAB AC link current can be expressed as a sum of harmonic sinusoids, viz

\[
i_p(w_{sw}t) = \sum_{n=1}^{\infty} i_p^m(w_{sw}t) = \sum_{n=1}^{\infty} i_p^m \sin(mw_{sw}t + \theta_p^m) \tag{7.1}
\]

The magnitude and phase angle of each of these harmonic components can be found by applying two-port network analysis to the 3-level modulation strategy for both converter bridges assuming negligible ripple in the DC bus voltage. The relationship between the AC link currents and the DAB switched bridge output voltages can thus be recalled from (3.4) for each harmonic component using AC phasor theory as

\[
\begin{bmatrix}
        I_p^m \angle \theta_p^m \\
        I_s^m \angle \theta_s^m
\end{bmatrix} = \frac{4V_{p,DC}}{\pi m} \begin{bmatrix}
        Y_{p,p}^m \angle \gamma_{p,p}^m & Y_{p,s}^m \angle \gamma_{p,s}^m \\
        Y_{s,p}^m \angle \gamma_{s,p}^m & Y_{s,s}^m \angle \gamma_{s,s}^m
\end{bmatrix} \begin{bmatrix}
        1 \angle \{m[\gamma/2]\} - 1 \angle \{m[-\gamma/2]\} \\
        d \angle \{m[\delta/2 - \delta]\} - d \angle \{m[-\delta/2 - \delta]\}
\end{bmatrix} \tag{7.2}
\]

where \(d\) is the DC-DC bus voltage ratio (incl. the transformer turns ratio \(N_p/N_s\)) and \(m = [2n - 1]\) with \(n = 1, 2, \ldots N\).

The primary bridge switching functions “crop” the harmonic AC link currents described by (7.1) into discontinuous segments on the DC bus, as shown in Fig. 7.2 for the first and third AC harmonic current components. These segments can then be expressed as another set of harmonic components using a Fourier series, giving a resulting DC bus current in harmonic form of
Figure 7.2: Translation from AC link to DC bus current harmonics in time domain

\[ i_{p,DC} = \sum_{k=0}^{\infty} c_k^h = \sum_{k=0}^{\infty} \frac{a_k^0}{2} + \sum_{k=1}^{\infty} \left\{ a_k^0 \cos(kw_{sw}t) + b_k^0 \sin(kw_{sw}t) \right\} \] (7.3)

From Fig. 7.2 it can be seen that a positive DC bus current component only flows during the period \(-\alpha/2 \leq wt \leq \alpha/2\) through switches \(S_{p,1}\) and \(S_{p,4}\), while a negative DC link current component only flows during the period \(\pi - \alpha/2 \leq wt \leq \pi + \alpha/2\) through switches \(S_{p,2}\) and \(S_{p,3}\). Using these limits, the harmonic co-efficients of (7.3) can be determined by a Fourier integral of the form

\[ I_{m,DC} = \int_{-\pi/2}^{\pi/2} i_{p,DC}(\omega_{sw}t) e^{j\omega_{sw}t} d(\omega_{sw}t) \] (7.4)

Substituting (7.1) into (7.4) gives

\[ c_k^h = \frac{1}{\pi} \left\{ \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} I_m \sin(mw_{sw}t + \theta_m^p) e^{jkw_{sw}t} d(\omega_{sw}t) - \int_{\pi - \frac{\pi}{2}}^{\pi + \frac{\pi}{2}} I_m \sin(mw_{sw}t + \theta_m^p) e^{jkw_{sw}t} d(\omega_{sw}t) \right\} \] (7.5)

which can be rearranged as

\[ c_k^h = \frac{1}{\pi} \sum_{n=1}^{\infty} I_m^p \left\{ \int_{\pi - \frac{\pi}{2}}^{\pi + \frac{\pi}{2}} \sin(mw_{sw}t + \theta_m^p) e^{jkw_{sw}t} d(\omega_{sw}t) - \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \sin(mw_{sw}t + \theta_m^p) e^{jkw_{sw}t} d(\omega_{sw}t) \right\} \] (7.6)

Using the relationship

\[ \sin \Delta = \frac{e^{j\Delta} - e^{-j\Delta}}{2j} \] (7.7)

(7.6) can be solved as
where and multiplying it by the (primary bridge) DC link voltage to get

\[
\begin{align*}
\zeta_p^{k(\text{odd})} &= 0 \\
\zeta_p^{k(\text{even})} &= \frac{1}{\pi} \sum_{n=1}^{\infty} I_p^n \left\{ \frac{[k-m][\cos(k-m)] \sin(\gamma_p^n) + \cos(\gamma_p^n)]}{\pi(k^2 - m^2)} \right\}
\end{align*}
\]

(7.8)

This reduces, for even \( k \), to

\[
\begin{align*}
a_k^p &= \sum_{n=1}^{\infty} I_p^n 2 \left[ \frac{\cos(\gamma_p^n)}{\pi(k^2 - m^2)} \right] \\
&= \frac{4}{\pi} \sum_{n=1}^{\infty} I_p^n \sin(\gamma_p^n) \begin{pmatrix} k \sin(\frac{\gamma_p^n}{2}) \cos(\frac{\pi}{2}) - m \cos(\frac{\gamma_p^n}{2}) \sin(\frac{\pi}{2}) \end{pmatrix} \\
b_k^p &= \sum_{n=1}^{\infty} I_p^n 2 \left[ \frac{\sin(\gamma_p^n)}{\pi(k^2 - m^2)} \right] \\
&= \frac{4}{\pi} \sum_{n=1}^{\infty} I_p^n \cos(\gamma_p^n) \begin{pmatrix} m \sin(\frac{\gamma_p^n}{2}) \cos(\frac{\pi}{2}) - k \cos(\frac{\gamma_p^n}{2}) \sin(\frac{\pi}{2}) \end{pmatrix}
\end{align*}
\]

(7.9a)

(7.9b)

Eqn. (7.9) defines the co-efficients of each of the harmonic components of the DC bus current that flows between the DC bus capacitors and the primary-side single phase bridge. From (7.8), it can also be concluded that the DC bus current contains only even harmonic multiples of the switching frequency, as could be expected since the odd switching harmonics of the modulation process convolve with the odd AC link current harmonics to produce only even DC bus harmonic components. The total harmonic distortion of the (primary) DC bus current then becomes

\[
THD_p = \sqrt{\frac{\sum_{l=1}^{\infty} (I_{p,DC}^l)^2}{I_{p,DC}^0}}, \quad k = [2l], l = 1, 2, 3, ...
\]

(7.10)

which is the DC equivalent of the AC link reactive power circulating current.

### 7.1.2 DC Power Transfer Relationship

A general expression for the power \( P_{p,DC} \) transferred between the DC source and the primary bridge can now be derived from (7.9) by setting \( k = 0 \) to select the DC current component, i.e.

\[
\begin{align*}
i_{p,DC}^0 &= \frac{a_p^0}{2} = \frac{2}{\pi} \sum_{n=1}^{\infty} I_p^n \sin(\frac{\gamma_p^n}{2}) \\
\end{align*}
\]

(7.11)

and multiplying it by the (primary bridge) DC link voltage to get

\[
P_{p,DC} = 2V_{p,DC} \cdot i_{p,DC}^0 = \frac{4V_{p,DC}}{\pi} \sum_{n=1}^{\infty} I_p^n \sin(\frac{\gamma_p^n}{2})
\]

(7.12)

where \( I_p^m \) and \( \theta_p^m \) are defined by (3.4) and vary depending on the values of \( \alpha, \beta \) and \( \delta \).

This relationship can be confirmed for a standard 2-level modulated DAB \((\alpha = \beta = \pi)\) with an ideal coupling inductance \( L \), i.e.

\[
\begin{align*}
Y_{p,p}^{m} &= Y_{p,p}^{m} - Y_{p,p}^{m} = \frac{1}{m w_{sw} L} \left\{ \cos(\frac{\pi}{2}) \right\} \\
Y_{p,a}^{m} &= Y_{p,a}^{m} - Y_{p,a}^{m} = \frac{1}{m w_{sw} L} \left\{ \sin(\frac{\pi}{2}) \right\}
\end{align*}
\]

(7.13)
Substituting these simplifications into (3.4) gives the phasor relationship of

\[ I_m \sin(\theta_m) \sin\left(\frac{m\pi}{2}\right) = \frac{8dV_{p,DC}}{m^2\pi\omega_{sw}L} \sin(m\delta) \]  

as illustrated in Fig. 7.3.

Figure 7.3: 2-level phasor diagram for ideal L

Further substituting (7.14) into (7.12), with \( \alpha = \pi \), gives

\[ P_{p,DC} = \frac{4dV_{p,DC}^2}{\omega_{sw}L} \sum_{n=1}^{\infty} \frac{8 \sin(m\delta)}{m^3} \]  

which, solving the summation series for \( |\delta| \leq \pi \), becomes

\[ P_{p,DC} = \frac{d(2V_{p,DC})^2}{\omega_{sw}L} \delta \left(1 - \frac{|\delta|}{\pi}\right) \]  

This result is identical to the power equation reported in [1] using piece-wise linear time domain analysis. Fig. 7.4 shows the normalised relationship between \( P_{p,DC} \) and the 3-level modulation control variables using (7.12) and (3.4) with discrete values of \( \delta \), for

- an idealised inductance (i.e. transformer with infinite magnetising inductance), Fig. 7.4(a),
- a transformer with reduced magnetising inductance and zero AC resistance, Fig. 7.4(b),
- an idealised inductance with significant series AC resistance, Fig. 7.4(c), and
- a transformer with reduced magnetising inductance and significant AC resistance, Fig. 7.4(d).

Each surface in these figures shows how the DC bus power transfer level changes for a constant \( \delta \) (each surface implies a specific value of \( \delta \in \{0, \pi/8, \pi/4, 3\pi/8, \pi/2\} \)) as the primary and secondary bridge duty cycles \( \alpha \) and \( \beta \) are varied. Note that for significantly resistive AC link impedance elements, the absolute primary and secondary DC bus power flow do not match due to the intermediate resistive losses. Also, if the DC-DC bus voltage ratio \( d \) moves further away from unity (i.e. \( d=1 \)), an active power transfer occurs even for non phase-shifted bridge output voltage patterns (i.e. \( \delta=0 \)) and 2-level modulation.
7.2 Three-Phase DAB

7.2.1 Fundamentals

Fig. 7.5 shows the matching topology for a three-phase DAB. Note that for a three-phase DAB, the three phase legs of each bridge are switched as a 120° displaced set of square waves, with the two sets of square waves phase shifted by \( \delta \) to control the power flow between the two bridges.

As already shown for the single phase DAB, the AC link currents flowing through each phase of
A similar process can now be used to determine the DC bus harmonics of a balanced three-phase DAB converter, with the topology and the modulation scheme shown in Fig. 4.1.

At each harmonic frequency (except for triplen harmonics), the phase leg output voltages form a balanced three-phase set with a zero magnitude star point voltage (as explained in Chapter 4). Hence the phase current harmonic components can be solved as a single phase equivalent circuit using AC phasor theory as before (except for triplen harmonics where no AC current flows), and expressed as

\[
\begin{bmatrix}
I_{m,p} \angle \theta_{m,p} \\
I_{m,s} \angle \theta_{m,s}
\end{bmatrix} = \frac{4V_{p,DC}}{\pi m} \begin{bmatrix}
Y_{m,p,p} \angle \gamma_{m,p,p} & Y_{m,p,s} \angle \gamma_{m,p,s} \\
Y_{m,p,p} \angle \gamma_{m,p,s} & Y_{m,s,s} \angle \gamma_{m,s,s}
\end{bmatrix} \begin{bmatrix}
1 \angle 0 \\
\text{d} \angle -m\delta
\end{bmatrix}_{m \neq \text{triplen}}
\] (7.18)

The DC bus current now becomes the summation of the “cropped” segments of these currents produced by the three-phase leg switching functions, which have an identical waveshape, but are phase shifted by \(2\pi/3\) and \(4\pi/3\) from phase leg 1 for phase legs 2 and 3 respectively. Hence the DC bus harmonic current will have the same form as (7.3), but with harmonic component co-efficients defined by

\[
L_p = a_p^h + jb_p^h = \frac{1}{\pi} \sum_{m=1}^{\infty} I_m^p \begin{bmatrix}
\int_0^{\pi/3} \sin(m\omega_{sw}t + \theta_{m,p}^p) e^{j\omega_{sw}t} d(\omega_{sw}t) \\
+ \int_{2\pi/3}^{\pi/3} \sin(m[\omega_{sw}t - 2\pi/3] + \theta_{m,p}^p) e^{j\omega_{sw}t} d(\omega_{sw}t) \\
+ \int_{4\pi/3}^{\pi/3} \sin(m[\omega_{sw}t - 4\pi/3] + \theta_{m,p}^p) e^{j\omega_{sw}t} d(\omega_{sw}t)
\end{bmatrix}
\] (7.19)
Note that the reference angle zero position has been changed from the single phase DAB waveform for consistency with Chapter 4. Also, triplen \( m \) can be excluded since no AC current flows for these harmonics. Again using (7.7), (7.19) can be solved as

\[
\begin{align*}
\epsilon_k &= \frac{1}{2\pi} \sum_{n=1}^{\infty} I_p \begin{cases}
\frac{e^{j\theta_m}}{|k+m|} & \text{for } k \geq m \\
\frac{e^{-j\theta_m}}{|k-m|} & \text{for } k < m
\end{cases}
\end{align*}
\]

which, recognising that \( m \) is always odd, produces non zero co-efficient values only for even and triplen \( k \), i.e.

\[
\begin{align*}
\epsilon_k &= \frac{3}{\pi} \sum_{n=1}^{\infty} I_p \begin{cases}
[k - m]e^{j\theta_m} - [k + m]e^{-j\theta_m} \\
[k - m]e^{j\theta_m} - [k + m]e^{-j\theta_m}
\end{cases}
\end{align*}
\]

(7.20)

(7.21)

which defines the co-efficients of the harmonic components of the DC bus current that flows between the DC bus capacitors and the primary side of a three-phase DAB. From (7.21) and (7.22), it can be seen that the DC bus current for a three-phase DAB contains only integer multiples of 6 with respect to the switching frequency, as could be expected by the nature of a balanced three-phase converter stage.

### 7.2.2 DC Power Transfer Relationship

A general expression for the power \( P_{p,DC} \) transferred between the DC source and a three-phase DAB primary bridge can be derived by setting \( k = 0 \) to select the DC current component and again multiplying it by the DC bus voltage, viz

\[
P_{p,DC} = 2V_{p,DC} \cdot i_0^{p,DC} = 2V_{p,DC} \cdot \frac{\theta}{2}
\]

(7.23)

Substituting the harmonic co-efficient from (7.22) gives

\[
P_{p,DC} = \frac{6V_{p,DC}}{\pi} \sum_{n=1}^{\infty} I_p \begin{cases}
\cos(\theta_m) & \text{for } m \text{ triplen} \\
\cos(\theta_m) & \text{for } m \text{ triplen}
\end{cases}
\]

(7.24)

This result can again be confirmed under the simplification of an ideal coupling impedance, to give

\[
I_p \cos(\theta_m) = \frac{4V_{p,DC}}{m^2\pi\omega_L} \sin(m\delta)
\]

(7.25)

Reflecting (7.25) into (7.24) gives

\[
P_{p,DC} = \frac{4V_{p,DC}^2}{\omega_L} \sum_{n=1}^{\infty} \sin(m\delta) \begin{cases}
6 & \text{for } m \text{ triplen} \\
6 & \text{for } m \text{ triplen}
\end{cases}
\]

(7.26)
The summation in (7.26) can be converted into a continuous (infinite) series summation by replacing \( \sin(m\delta) \) for non-triplen \( m \), with

\[
\frac{1}{3} \left\{ \begin{array}{l}
3\sin(m\delta) \\
-\sin(m\delta) - \sin(m[\delta - \frac{2\pi}{3}]) - \sin(m[\delta - \frac{4\pi}{3}])
\end{array} \right\}_m
\] (7.27)

Hence (7.26) can be expressed as

\[
P_{p,DC} = \frac{4dV_{p,DC}^2}{\omega_{sw} L} \sum_{n=1}^{\infty} \frac{2\sin(m\delta)}{n^2m^3} - \frac{\sin(m[\delta - \frac{2\pi}{3}])}{n^2m^3} - \frac{\sin(m[\delta - \frac{4\pi}{3}])}{n^2m^3}
\] (7.28)

Taking into account periodicity and absolute value considerations for the two regions of \( |\delta| \leq \frac{\pi}{3} \) and \( \frac{\pi}{3} < |\delta| \leq \frac{\pi}{2} \), (7.28) can be reduced to

\[
P_{p,DC} = \begin{cases} 
\frac{d(2V_{p,DC})^2}{\omega_{sw} L} \delta \left( \frac{2}{3} - \frac{|\delta|}{\pi} \right) & \text{for } |\delta| \leq \frac{\pi}{3} \\
\frac{d(2V_{p,DC})^2}{\omega_{sw} L} \delta \left( 1 - \frac{|\delta|}{\pi} - \frac{|\delta|}{\pi|n|} \right) & \text{for } \frac{\pi}{3} < |\delta| \leq \frac{\pi}{2}
\end{cases}
\] (7.29)

which is identical to the power equation reported in [1] using piece-wise linear time domain analysis.

### 7.3 Summary

This chapter has extended the fundamental AC link analysis in Chapters 3 and 4 to quantify the magnitude of the harmonic frequencies in the DC bus output current, subject to the DC-DC bus voltage ratio, the AC link impedances and the modulation parameters. The zero order DC bus harmonic is then used to express generic power transfer relationships for a single and three-phase DAB.
8 Active Suppression of DC Bus Harmonics

The analysis of the DC bus current harmonics in Chapter 7 is now used to address the practical issues in the DC bus filter design that can lead to harmonic problems such as excessive electromagnetic interference (EMI), significant filter stress and eventual component failure. Conventionally, the relatively large DC bus filter capacitor (or inductor) that is normally used in a DAB helps to suppress these DC bus dynamics by creating a reasonably low filter cut-off frequency. However, the use of adaptive 3-level modulation for a single phase DAB provides a much greater solution space to achieve a desired power transfer condition, with the three PSSW control angles that are available. This chapter now explores the additional use of these angles to selectively suppress particular DC bus current harmonics across the entire operating range of the converter as an alternative approach reducing the filter capacitor size to the minimum value required to support the bridge switching transitions, with low-order modulation harmonics absorbed by the terminating impedance (e.g. a battery or an external bulk capacitive element) without creating a resonance hazard. This new active harmonic suppression (AHS) strategy is validated by theory, simulation and matching experimental results.

8.1 Bridge Filter Capacitor and Parasitic Resonant Circuit

Fig. 8.1(b) shows a typical physical arrangement for such a bridge, where the parasitic inductance \( L_{DC} \) created by the wiring connection from the bulk DC electrolytic capacitors (2x Kendeil KO1450222, paralleled) via the DC bus capacitor (1x Kemet 463R4100) to the DC tabs of the phase leg module can be clearly seen. Fig. 3.1(c) shows the 3-level PSSW modulation strategy that is used to modulate the DAB, where each phase leg is switched with a square wave, the primary and secondary bridge phase leg square waves are displaced by \( \alpha \) and \( \beta \) respectively to produce reduced magnitude bridge output voltages, and the two bridge output voltages are displaced by \( \delta \) to control the power flow (\( \delta \): load angle).

From Fig. 8.1(a), it can be seen that the DC bus current harmonics will share between the high-frequency bus capacitor branch \( R_{ESR}/C_{DC} \) and the parasitic inductance connection \( R_{DC}/L_{DC} \) to the external source according to Kirchoff’s current law. Hence the harmonic currents that flow into the external source from DC bus harmonics injected into the DC bus by the phase leg, are given by (for an ideal external voltage source with \( C_{src} \to \infty \))

---

Material in this chapter was first published in:
The high-frequency bus capacitor current harmonics can similarly be determined as

\[
I_{\text{cap}}^k \theta_{\text{cap}}^k = G_{\text{tf}, \text{cap}}^k \theta_{\text{cap}}^k \cdot I_{\text{p,DC}}^k \theta_{\text{p,DC}}^k \quad \text{where}
\]

\[
G_{\text{tf}, \text{cap}}^k \theta_{\text{cap}}^k = \frac{1 + jk \omega_0 R_{\text{ESR}}^k C_{\text{DC}}}{1 - (k \omega_0)^2 L_{\text{DC}} C_{\text{DC}} + jk \omega_0 C_{\text{DC}} (R_{\text{DC}}^k + R_{\text{ESR}}^k)}
\]  

The second order denominator of (8.1) and (8.2) clearly identifies an oscillation hazard if the resonant frequency of the DC side impedance is close to a DC bus current harmonic component of significant magnitude. Note that the parasitic inductance in \(L_{\text{DC}}\) as well as any passive damping caused by the parasitic resistance \(R_{\text{DC}}\) may be difficult to determine at the design stage, and hence identifying a DC bus resonant frequency \(f_{\text{DC, res}}\) hazard before experimental testing can be very challenging.

Fig. 8.2 presents Bode plots for the DC filter frequency characteristic \(G_{\text{tf}, \text{arc}}^k \theta_{\text{arc}}^k\) of the exemplar physical bridge (parameters listed in Table 8.1), for increasing values of DC bus bridge capacitance and a constant parasitic DC bus inductance of 200 nH connecting to the external power source. The damping resistances \(R_{\text{DC}}\) and \(R_{\text{ESR}}\) were estimated by developing a PLECS simulation [130] that matched the experimental response shown later in Fig. 8.3 and Fig. 8.4, with (frequency-independent) values of
CHAPTER 8. ACTIVE SUPPRESSION OF DC BUS HARMONICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary bridge...</td>
<td></td>
</tr>
<tr>
<td>... DC bus inductance (parasitic)</td>
<td>$L_{DC}$</td>
</tr>
<tr>
<td>... DC bus capacitance</td>
<td>$C_{DC}$</td>
</tr>
<tr>
<td>... bulk source capacitance</td>
<td>$C_{src}$</td>
</tr>
<tr>
<td>AC link coupled inductor</td>
<td>$L$</td>
</tr>
<tr>
<td></td>
<td>$R$</td>
</tr>
<tr>
<td>Primary DC bus voltage</td>
<td>$2V_{p,DC}$</td>
</tr>
<tr>
<td>DC-DC bus voltage ratio</td>
<td>$d$</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>$f_{sw}$</td>
</tr>
</tbody>
</table>

Table 8.1: AC link, DC bus impedances and DAB operating conditions

$R_{DC}^k=R_{DC}=25$ mΩ and $R_{ESR}^k=R_{ESR}=30$ mΩ. Note that $R_{ESR}$ is reduced linearly inverse to $C_{DC}$ as can typically be observed in practice [132].

The enhanced vertical lines in the Bode diagrams show the locations of the even integer harmonics of the fundamental PSSW switching frequency (20 kHz), as have been analytically determined in the previous chapter. Note that these DC side current harmonics are all even (e.g. 40 kHz, 80 kHz, 120 kHz etc.) because the rectification action of each H-bridge causes a fundamental frequency shift from the odd PSSW AC side current harmonics (e.g. 20 kHz, 60 kHz, 100 kHz, etc.). In principle, the effect of any critical DC bus resonance that may occur can be suppressed by one of the two following approaches:

Figure 8.2: Bode plot of prim. bus transfer function for variable bridge capacitance ($L_{DC} = 200$ nH)
• Passive Damping: The bridge capacitor value $C_{DC}$ is selected as large as is required to suppress all relevant DC bus harmonic frequencies. For example, for the reference bridge impedance parameters and operating conditions shown in Table 8.1, $C_{DC}$ has to be at least 100 $\mu$F, as shown in Fig. 8.2(a). This may not only be difficult to physically achieve without creating a further parasitic inductive connection, but also means that the 2$^{\text{nd}}$ harmonic DC bus current component will still flow (almost) one-to-one to the terminating source supply (for $C_{DC}$=100 $\mu$F). Alternatively, a separate discrete DC bus filter inductor can be added to reduce the resonant cut-off frequency of the parasitic $LC$ resonant circuit, which can be useful to reduce the total filter volume if the injected bridge DC harmonic magnitudes are low relative to the DC bus voltage (as happens in higher voltage lower current applications). In any case, passive damping is a relatively ad hoc approach that is difficult to design, and may not be effective in many applications.

• Active Harmonic Suppression (AHS): If $C_{DC}$ is set significantly less than 100 $\mu$F, the parasitic DC bus resonance will inevitably be excited by one of the injected DC bus current harmonics. For $C_{DC}$ =10 $\mu$F, the rather significant 6$^{\text{th}}$ DC bus harmonic is likely to cause substantial DC bus oscillations, as indicated by Fig. 8.2(b). Unfortunately, since this harmonic multiple is a convolution product of two low-order AC link current harmonic components which contribute significantly to the zero order DC bus harmonic and thus the fundamental power transfer, it is difficult to suppress using AHS. Reducing $C_{DC}$ further to 1 $\mu$F causes a resonance at the less significant 18$^{\text{th}}$ harmonic frequency as shown in Fig. 8.2(c), which is easier to suppress using AHS as will be presented later. As the DC bus capacitance is reduced further, i.e. $C_{DC}$=0.5 $\mu$F in Fig. 8.2(d), the parasitic resonant frequency becomes higher and higher, and hence is less likely to be influenced by DC bus harmonics injected from the DAB switching process. However, a certain minimum bridge capacitance is always required to buffer energy for the bridge switching transitions, which limits the minimum size DC bus capacitance that is feasible. For the AHS approach, the lower-order DC bus current harmonics (below the parasitic resonance cut-off frequency) created by the PSSW modulation process will be absorbed by the external source (e.g. a battery [133] [134]).

8.2 Simulation and Experimental Verification of DC Bus Oscillations

To illustrate the potential DC resonance hazard for a DAB converter, the DC bus capacitors for both the primary and secondary side bridge of the exemplar DAB with parameters as listed in Table 8.1, were set to $C_{DC}$=1 $\mu$F. The AC link coupling impedance network was simplified to an $RL$ coupled inductor component (i.e. single AC link current path and “unity transformer turns ratio”), whereby the matrix elements of $[Y]$ for the two-port analysis follow (3.13)

Fig. 8.3(a) and (b) (OP1), and Fig. 8.4(a) and (b) (OP3), illustrate the DC bus oscillation that...
occurs (both in simulation and in matching experimental conditions) for this converter under two exemplar operating conditions, where a significant $18^\text{th}$ harmonic resonance current (dominant: $f_{\text{DC, res}} = 360$ kHz) is measured in the DC bus current that flows back into the external source. The phase angle drift of source current harmonic frequencies causes the ring to decay within a half primary switching cycle. It is commented that this oscillation becomes more severe as the output current magnitude increases in relation to the DC bus voltage. Note also that the results from simulation and experiment slightly differ due to frequency dependencies, the actual IGBT voltage drop and some DC bus voltage oscillation across the secondary bridge output voltage.
8.3 Elimination of Primary DC Bus Oscillation

Active Harmonic Suppression (AHS) will now be used to suppress the critical DC bus current oscillation around the dominant 18th harmonic. Fig. 8.5(a) shows the magnitude of this 18th harmonic current component \( i_{18, p, DC} \) as \( \alpha \) and \( \delta \) vary, while \( \beta \) is kept constant at \( \pi \), for average DC bus currents of 1.6 A and 1.9 A feeding into the DAB (determined for \( N=30 \)). Note that ZVS operation is maintained for all operating conditions in accordance with the principles of Chapter 3, indicated as solid filled symbols. From this figure, it can be seen that for \( \alpha = 2.95 \) (radians) the 18th DC bus current harmonic component is heavily suppressed. This suggests that if the DAB is always operated with this value for \( \alpha \) as the power magnitude varies between these two reference levels, the unacceptable 18th harmonic resonance in the DC bus current should be significantly reduced.

As a practical aspect it is noted here that Polypropylene (PP) film capacitors are typically available with a positive/negative tolerance of 5 – 10\% [132]. Similar deviations can be expected for the parasitic DC bus inductance (of e.g. a battery cable). A relative component tolerance in either \( C_{DC} \) (tol\( C \)) and/or \( L_{DC} \) (tol\( L \)) causes a relative change in resonance frequency (tol\( f_{res} \)) of \[ \text{tol} \( f_{res} \) = \frac{1}{\sqrt{(1+\text{tol} C)(1+\text{tol} L)}} - 1. \]

For the worst-case condition, i.e. a maximum deviation of 10\% at the same negative (positive) polarity,
CHAPTER 8. ACTIVE SUPPRESSION OF DC BUS HARMONICS

Figure 8.6: PSSW modulation angles to minimise impact of 18th DC bus harmonic while maintaining ZVS (exemplar MATLAB script shown in Appendix D)

tol \_f\_res becomes +9% (-11%). Hence, for this application example, the primary DC bus resonance peak would be located anywhere between the 16th and the 20th harmonic. Fig. 8.5(b) then shows how the magnitude of the neighboring DC bus harmonics (16th, 20th) varies as \( \alpha \) and \( \delta \) vary. It can be observed that while their minimums are located slightly apart from OP2, their magnitudes are however still largely suppressed for this operating condition. Hence the AHS technique retains its suppressing capability to a large extent despite practical component tolerance variations (or low Q filter resonant circuits).

Fig. 8.6 then shows the PSSW modulation angles to minimise the magnitude of this particular harmonic for the entire power range of the exemplar converter. Note that for small load angles, i.e. partial load conditions, \( \alpha \) needs to be reduced to maintain ZVS soft switching operation of all DAB phase legs at the given DC-DC bus voltage ratio \( d \) of 0.8 (as a result of the analysis in Chapter 3).

8.3.1 Large Load Angle

The experimental single phase DAB system is now used to verify this concept and to show how the harmonic components that excite the characteristic DC bus resonant frequency can be actively suppressed using adaptive 3-level modulation while still maintaining constant power transfer. Fig. 8.7(a) and Fig. 8.7(b) (OP2), and Fig. 8.8(a) and Fig. 8.8(b) (OP4), provide simulation and experimental confirmation of this result. The elimination of the 18th component is also shown in the harmonic spectrum of Fig. 8.7(c) and Fig. 8.8(c) respectively. As anticipated by Fig. 8.5(b), the waveforms consequently show a significant suppression of the 18th and any surrounding harmonic current components (“notch filter”) in the external supply current if the PSSW mitigation process is centered about the estimated parasitic DC bus resonance frequency.

8.3.2 Small Load Angle

Fig. 8.9 shows matching results for a reduced load angle, i.e. low load condition, confirming the generality of the AHS resonant damping concept using interactive adjustment of \( \alpha \) and \( \delta \). Note that in this case, \( \alpha \) is reduced from 2.95 (radians) to maintain ZVS operation of the secondary bridge with a
8.4 Elimination of Primary and Secondary DC Bus Oscillation

Fig. 8.10 shows the selective AHS of the 18th harmonic in the primary DC bus for an average input current of 1.3 A. However, the ring in the experimental secondary bridge output voltage waveform $v_s$ indicates that the physical arrangement of the secondary DC bus causes another DC bus resonance at the 10th harmonic (dominant: $f_{DC, res} = 200$ kHz). The secondary (physically longer rail) DC bus voltage ratio of $d = 0.8$. 

DC bus voltage ratio of $d = 0.8$. 

Figure 8.7: Adaptive PSSW @ 1.9 A (OP2: $\alpha = 2.95, \delta = 0.82$)

Figure 8.8: Adaptive PSSW @ 1.6 A (OP4: $\alpha = 2.95, \delta = 0.64$)
bus inductance was therefore determined to be 650 nH for the same bridge capacitor value of 1 µF \((R_{DC}^{k}=100 \, \text{mΩ}, \, R_{ESR}^{k}=30 \, \text{mΩ})\). The Bode plot of the corresponding \(LC\) transfer function in Fig. 8.11 in combination with the spectrum of injected DC bus current harmonics in Fig. 8.10(c) confirm this observation.

Using the selective harmonic suppression strategy for the primary and the secondary DAB converter bridge, this secondary side DC bus resonance can be suppressed simultaneously by varying the secondary side bridge duty cycle \(\beta\). Fig. 8.12 shows a smoothed secondary bridge voltage waveform, which

---

**Figure 8.9:** Adaptive PSSW @ 0.4 A \((\alpha = 2.30, \, \delta = 0.17)\)

**Figure 8.10:** Adaptive PSSW @ 1.3 A \((\alpha = 2.95, \, \beta = \pi, \, \delta = 0.48)\)
8.4. ELIMINATION OF PRIMARY AND SECONDARY DC BUS OSCILLATION

Figure 8.11: Bode plot of secondary DC bus transfer function

Figure 8.12: Adaptive PSSW @1.3 A (α = 2.95 rad, β = 2.60 rad, δ = 0.52 rad)

confirms the capability to also mitigate the secondary side DC bus harmonic currents (here: β = 2.60). Note however that the simultaneous suppression of particular harmonic currents in both DC buses can significantly constrain the power transfer capability and ZVS operation of the DAB. Hence hard switching may be unavoidable for certain DC-DC bus voltage ratios and load conditions (as can be observed in Fig. 8.12(a) where the devices in phase leg HB4 experience hard turn-ON events). For this particular application example, it may thus be more attractive to passively suppress the secondary DC bus oscillation by e.g. using a larger bus capacitor (50 - 100 µF). These influences generally add more significant constraints if lower order parasitic resonance frequencies are being suppressed by adaptive 3-level modulation. In this context it is also mentioned that for DAB converters with a significant voltage boost ratio and winding turns ratio (in case of an actual high-frequency AC link transformer), the AHS is preferably applied at the lower voltage DC bus/converter bridge if the voltage drop across the DC bus $R_{DC}/L_{DC}$ impedance - particularly at twice the fundamental frequency - is moderately low.
It should be recognised that the AHS approach reduces the control degrees of freedom provided by the 3-level DAB modulation concept which could otherwise be used to maximise the conversion efficiency at every operating point. In Chapter 6, the primary objective is to set the modulation parameters to reduce the AC link RMS circulating currents, i.e. achieve an overall reduction of the (reactive power) harmonic distortion in the DC bus current, and maintain ZVS as the operating conditions vary. In contrast, the control strategy presented in this chapter aims to suppress a particular resonant frequency in the DC bus currents for all operating conditions.

Another important loss aspect about AHS however is its potential to avoid additional heat dissipation in the DC bus components (e.g. capacitors) that would otherwise result from an un-damped DC bus current oscillation. Ref. [132] shows typical impedance and ESR measurements for a wide range of metallized film PP capacitors across frequencies from kHz to MHz. For example, for the considered prototype converter and the operating conditions shown in Figs. 8.3 and 8.4, the excited DC bus resonance more than doubles the total filter network losses, compared to using AHS with the resulting reduced DC bus current oscillation as shown in Figs. 8.7 and 8.8.

8.5 Summary

After identifying the harmonic problems that can be caused by the DAB modulation process and resonant DC bus impedances, this chapter has shown how adaptive 3-level modulation can be used to actively shape the DC bus current and selectively suppress particular harmonic components that cause critical frequency resonance DC bus oscillations across the entire operating range. This strategy also allows to reduce the filter size of a DAB compared to a conventional passive damping design approach.
9 Experimental System and Simulation Environment

This thesis has introduced a new harmonic analysis strategy for DAB converters. All conclusions and concept creations have been carefully verified in both simulation and experimental work to support the analytical investigations. This chapter now describes the simulation environment and the experimental laboratory prototypes used to support and validate this work. It is commented here (again) that the specification details of the customised DAB prototype in Chapter 6 have not been disclosed in this thesis due to IP ownership of the industry partner (only few descriptive words are mentioned within the context of the efficiency evaluation). Instead, an existing DAB prototype was provided by the RMIT laboratory which has been modified in the course of this thesis to illustrate and validate the theoretical principles.

9.1 Experimental System

Fig. 9.1 describes the laboratory setup used for both single and the three-phase DAB. The experimental DAB power converter is the core element and device under test. It comprises the basic DAB hardware (i.e. IGBT bridge connections, filter capacitors, etc.) and has sufficient capacity to operate the selected DAB systems at power levels below 1 kW for a DC bus voltage range between 20 V and 250 V at either DC bus terminals.

While this basic device setup has been consistently used in the course of this work, the AC coupling impedances connected to the IGBT phase leg AC outputs were varied as necessary for best possible
illustration of individual effects. The DC buses of the experimental DAB power converter were energised by standard DC power supplies to provide a stiff DC source voltage for stable operation, with paralleled (resistive) load banks to allow energy to be absorbed at the receiving bridge. Measurement devices are connected to the power devices of interest to record the current and voltage data on a 4-channel oscilloscope. A computer station allows to communicate to the control board via an RS485 Modbus protocol.

9.1.1 Power Stage

Single Phase DAB

Fig. 9.2 provides a side and a top view of the experimental single phase power stage including its control board. The DAB rig employs two H-bridge converters that each connect to one termination port of the AC link impedance network. Each H bridge is constructed using two BSM75GBN60 IGBT modules (discrete package: IKW75N60T). All four IGBT modules are mounted on top of the same aluminum heatsink. The two modules of one H bridge are hard connected through a positive and negative DC bus copper bar, which also accommodates the bus bar bolted DC bus capacitors. Fig. 9.3 shows how these fast polypropylene (PP) film capacitors are integrated right across the switch modules, necessary to support the DC bus voltage at the location of the IGBT modules and to reduce the commutation loop and stray inductance of a switching event for all phase legs (HB1 - HB4). Both power and signal circuits have been designed to comfortably operate the DAB at 20 kHz.

The power circuit includes an external relay contactor for over-current protection at the primary DC output port. Large electrolytic capacitors on either DC bus are hard wired to the respective DC bus bars. Table 9.1 lists the major power circuit devices.

<table>
<thead>
<tr>
<th>Component</th>
<th>Model</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Phase leg modules</td>
<td>2 x Infineon BSM75GBN60</td>
<td>IGBT-based estimated parasitic commutation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>inductance: $L_{par} = 15 \text{ nH} - 25 \text{ nH}$</td>
</tr>
<tr>
<td>Gate driver IC</td>
<td>HCPL-316J</td>
<td>$U_{GE, \text{off}} = -5.0 \text{ V}, R_{G, \text{off}} = 4.7 \text{ Ω}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$U_{GE, \text{on}} = 17.0 \text{ V}, R_{G, \text{on}} = 10.0 \text{ Ω}$</td>
</tr>
<tr>
<td>DC bus capacitors</td>
<td>4 x Vishay MKP1848C61010</td>
<td>10 μF, 1000 VDC Polypropylene</td>
</tr>
<tr>
<td></td>
<td>Kemet 463R4100</td>
<td>(in Chapter 6: paralleled 100 μF cap.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 μF, 630 VDC Polypropylene</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(exclusively used in Chapter 8)</td>
</tr>
<tr>
<td>DC bulk source capacitors</td>
<td>2 x Kendeil KO1450222</td>
<td>2.2 mF, 450 VDC Electrolyte</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(primary: parallel-connected)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(secondary: series-connected)</td>
</tr>
<tr>
<td>DC power supplies</td>
<td>MagnaPower (current-limited)</td>
<td>High voltage: 250V/11.6 A,</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High current: 40V/50A</td>
</tr>
</tbody>
</table>

Table 9.1: Power stage (per bridge)
Figure 9.2: Experimental single phase DAB converter rig
Three-Phase DAB

The three-phase converter rig is shown in Fig. 9.4. It employs three phase leg modules per converter bridge. Two separate control boards have been synchronized in a master-slave configuration to create a six-step modulation pattern from each bridge output, and avoid a drift in the gate signals of one bridge with respect to the other. Power and signal circuits have been designed to comfortably operate the rig at 5 kHz.
9.1.2 Magnetics

The presented work has explored various kinds of custom-made coupled inductors and transformers to verify the analytical results. This section lists their design specifications.

**Design A: Single Phase Coupled Inductor**

Fig. 9.5 shows the single phase inductor used as coupling impedance in Chapter 3 (CM: common-mode) and Chapter 5 (DM: differential-mode). For common-mode excitation, the main core flux is induced by both coils in the same direction, whereas for differential-mode excitation, the core flux is canceled and only the flux in the air (i.e. the total equivalent transformer leakage inductance) remains. The design specifications are listed in Table 9.2. The impedances were measured across a wide frequency range from 20 kHz to 100 kHz using an impedance analyser. The negative change in the leakage inductance is very minor (≤ 5%). The coupled inductor has been designed in a way such that the impact of the AC resistance (and its higher-order harmonic resistance parameters) is rather negligible in both CM and DM configuration for a fundamental operating frequency of 20 kHz.

<table>
<thead>
<tr>
<th>Geometry</th>
<th>Core</th>
<th>Impedances</th>
</tr>
</thead>
</table>
| Core     | 1x U-core (TDK B67345B0010X087)  
1x I-core (TDK B67345B0011X087)  
Material: N87 ferrite  
Gap: 1.7 mm | $L_{CM}$  
$530 \mu\text{H}$  
$L_{DM}$  
$103 \mu\text{H}$  
$R_{CM} \approx R_{DM}$  
$0.4 \Omega$ |
| Coil     | Two identical bobbins  
Turns ratio: 1:1  
Each winding: 4 layers x 5 turns  
Litz wire: 19x 0.7mm strands  
(3 wires in parallel) |

Table 9.2: Design A: Specifications (fundamental frequency: 20 kHz)
Design B: Variable-Type Single Phase Transformer

Design A was modified to create a high-frequency transformer with a finite magnetising inductance to analyse its impact on the ZVS region. The geometry of the primary and secondary coil are not designed identically to achieve a varying flux relationship for a unity transformer turns ratio. In addition, the airgap dimension can be altered between two values and the position of the primary coil is flexible (around the core edge or around the core gap). This results in four different impedance combinations (T1-T4) as sketched in Fig. 9.6. Table 3.1 shows the measured inductance parameters for T1-T4. Table 9.3 summarises the core and coil geometry. Note that the transformer is designed such that the AC resistance is negligible with respect to the series inductance.

<table>
<thead>
<tr>
<th>Geometry</th>
<th>Core</th>
<th>Material: N87 ferrite</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2x U-core (TDK B67345B0010X087)</td>
<td></td>
</tr>
<tr>
<td>Coil</td>
<td>Two bobbins</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Turns ratio 1:1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Prim.: 2 layers x 8 turns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sec.: 1 layers x 16 turns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Litz wire: 19x 0.7mm strands</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(1 wire in parallel)</td>
<td></td>
</tr>
</tbody>
</table>

Table 9.3: Design B: Specifications (fundamental frequency: 20 kHz)

Figure 9.6: Magnetic design B (left: primary, right: secondary)
Design C: “Three-phase” Transformer

In order to validate the three-phase DAB analysis in Chapter 4, three identical single phase coupled inductors were wound, as shown in Fig 9.7, and connected as a three-phase transformer equivalent with floating star point connection. For this transformer design, the leakage inductance was measured to slightly reduce ($\approx 15\%$) from 5 kHz to 55 kHz, while the AC resistance is significant but essentially constant in the considered frequency range. For the unbalanced three-phase impedance, the turns count of the phase 2 transformer coils were reduced to approximate the practicality of an asymmetric three-phase transformer design geometry. The design specifications are listed in Table 9.4.

<table>
<thead>
<tr>
<th>Geometry</th>
<th>Core</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2x C-core (BFi OptiLAS AMCCC-63)</td>
</tr>
<tr>
<td></td>
<td>Material: Iron-based amorphous alloy ($B_{sat} = 1.56$ T)</td>
</tr>
<tr>
<td></td>
<td>Gap $&lt; 0.6$ mm</td>
</tr>
<tr>
<td>Coils (balanced)</td>
<td>Two identical bobbins</td>
</tr>
<tr>
<td></td>
<td>Turns ratio 1:1</td>
</tr>
<tr>
<td></td>
<td>Each winding: 2.8 layers x 13 turns</td>
</tr>
<tr>
<td></td>
<td>Litz wire: 19x 0.7mm strands (2 wires in parallel)</td>
</tr>
<tr>
<td>Coils (unbalanced)</td>
<td>Two identical bobbins</td>
</tr>
<tr>
<td></td>
<td>Turns ratio 1:1</td>
</tr>
<tr>
<td></td>
<td>Each winding: 2.0 layers x 13 turns</td>
</tr>
<tr>
<td></td>
<td>Litz wire: 19x 0.7mm strands (2 wires in parallel)</td>
</tr>
<tr>
<td>Phase impedances</td>
<td></td>
</tr>
<tr>
<td>(balanced)</td>
<td>$L_{DM} = L_{\sigma, \text{tot}}$</td>
</tr>
<tr>
<td></td>
<td>$L_{CM} \approx 4L_{in}$</td>
</tr>
<tr>
<td></td>
<td>$R$</td>
</tr>
<tr>
<td></td>
<td>250 $\mu$H</td>
</tr>
<tr>
<td></td>
<td>7.7 mH</td>
</tr>
<tr>
<td></td>
<td>1.2 $\Omega$</td>
</tr>
<tr>
<td>Phase 2 impedance</td>
<td></td>
</tr>
<tr>
<td>(unbalanced)</td>
<td>$L_{DM(\text{mod.})} = L_{\sigma, \text{tot(\text{mod.})}}$</td>
</tr>
<tr>
<td></td>
<td>$R_{DM(\text{mod.})}$</td>
</tr>
<tr>
<td></td>
<td>125 $\mu$H</td>
</tr>
<tr>
<td></td>
<td>0.8 $\Omega$</td>
</tr>
</tbody>
</table>

Table 9.4: Design C: Specifications (fundamental frequency: 5 kHz)
9.1.3 DSP board

The power stage IGBTs were turned ON and OFF using isolated gate drivers whose input signals were fed by a control board provided by Creative Power Technologies [135]. The control board comprises a Switched Mode Power Supply (SMPS) and a separate DSP board as shown in Fig. 9.9: it employs a TMS320F2810 Digital Signal Processor (DSP) manufactured by Texas Instruments and is hard wired to a USB adapter board which provides the external read and write functionality to adjust the Phase Shifted

Figure 9.8: Exemplar micro-controller implementation of PSSW modulation through common carrier
Square Wave (PSSW) modulation angles required for open-loop operation of the DAB as illustrated in Figs. 9.1 and 9.2.

The DSP calculates the individual bridge phase leg transition time by comparison of a common triangular carrier wave with each phase leg’s square wave reference. This process is illustrated in Fig. 9.8(a). In Fig. 9.8(b) a positive phase shift is applied between the reference phase leg’s complementary gate signals and any other phase leg’s complementary gate signals, by modifying the magnitude of the reference square wave (magnitude equals zero for HB1) which is then compared to a common triangular carrier waveform as is well known from Pulse Width Modulation (PWM) theory. To create a negative phase shift, this square wave is inverted as illustrated in Fig. 9.8(c). The carrier-reference comparsion creates the gate signal pulse patterns shown at the bottom of each subfigure. A variable magnitude of the reference square wave produces variable (positive or negative) phase shifts up to 90°. For larger phase shifts (e.g. for HB2), the gate signal output of that respective phase leg can be reversed to achieve a 180° bias offset phase shift. The gate drivers convert these pulse patterns into physical gate voltage transitions at the switch device input, by injecting/drawing charge into/from the IGBT gates. The turn-ON instant of the incoming switch must always be delayed with respect to the turn-OFF of the opposite switch pair element of the same phase leg. This dead-time interval is kept constant during converter operation.

9.1.4 Measurement Equipment

The major measurement devices for this work are listed in Table 9.5.

<table>
<thead>
<tr>
<th>Device</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscilloscope</td>
<td>Agilent Technologies MSO7014A 100 MHz</td>
</tr>
<tr>
<td>High Voltage Differential Probe</td>
<td>Tektronix P5200</td>
</tr>
<tr>
<td>AC/DC Current Probe</td>
<td>Tektronix TCPA300</td>
</tr>
<tr>
<td>Impedance analyser</td>
<td>WayneKerr 6500B</td>
</tr>
<tr>
<td>Power analyser</td>
<td>ZIMMER LMG 500</td>
</tr>
</tbody>
</table>

Table 9.5: Measurement equipment
9.2 Simulation Environment

A separate simulation environment has been established. PLECS 3.4.6 Toolbox [130] for MATLAB Simulink was used to model the investigated DAB converter systems prior to the experimental work. Fig. 9.10 shows the high level Simulink schematics for a single phase DAB (and similar for a three-phase DAB). They mainly comprise a modulator block (programmed in Simulink) and a PLECS circuit. The modulator block is fed by the three modulation angles $\alpha$, $\beta$ and $\delta$ in accordance to their definition in this thesis. The DC-DC voltage ratio is forwarded to the PLECS circuit, while the primary DC bus voltages, the AC link and DC bus impedances as well as the carrier switching frequency and dead-time period are initialised in MATLAB. The PLECS schematics are aligned with the circuits shown in Figs. 3.1, 4.1 and 7.1 depending on the scope of interest ($RL$ coupled inductor, single phase or three-phase HF transformer, (non-)stiff DC bus, etc.). After each simulation run, the most characteristic AC link and DC bus voltage and current waveforms are exported to MATLAB for the plotting analysis. It is also commented here that the simulation environment provides exactly matching results for the harmonic analysis with the full-order numerical summation calculations (neglecting frequency dependencies that can only be readily accommodated by the harmonic analysis). Other second-order effects (e.g. IGBT device voltage drop) and large signal impedance variations (e.g. variation of the ferrite core permeability with excitation and temperature) however may cause the simulation and analytical results to slightly differ from the experimental observations.

The selected experimental system and the simulation environment have been presented throughout the thesis to confirm the analytical developments and the proposed impedance design or modulation concepts.
Figure 9.10: MATLAB Simulink block schematics for single phase DAB
9.2 SIMULATION ENVIRONMENT

Figure 9.11: PLECS circuit
10 Conclusion and Future Work

10.1 Conclusion

Precisely identifying the ZVS boundary conditions of a Dual Active Bridge (DAB) DC-DC converter for any design and operating context is key to minimising the switching energies that need to be dissipated at reasonable effort. Simultaneously however, this change will cause the practicalities of the AC link coupling network (in particular the transformer) and the non-ideal switching process to become more relevant in the entire design process. These effects have to be readily included into the analysis to accurately determine the available ZVS operating range. However, a DAB is conventionally designed using time domain analysis which presumes an idealized single parameter AC link inductance to characterise the modulation and power device waveforms and thus evaluate the ZVS condition of a DAB. Such an analysis technique only approximates the more complex model of a practical DAB high-frequency AC link, and as consequence it does also not allow the designer to account for more complex network impedance structures.

This thesis presents a new harmonic analysis technique to better manage advanced design and operational concepts for a DAB. It verifies the wide applicability of this approach, and utilises the developed solution strategy to precisely describe the interaction between the PSSW modulation and the AC link or DC bus impedances of a DAB. Chapters 3 and 4 present a new theoretical approach using harmonic analysis to analytically determine the ZVS boundary conditions of both single and three-phase DAB converters across the entire range of operating conditions. These are then used to accurately determine the ZVS boundaries for any particular DAB design and operating context, by identifying the precise relationship between the modulation angles and the bridge DC bus voltage levels. This analysis technique allows more complex bridge coupling networks, and non-ideal switching effects and advanced modulation strategies to be readily included. Numerical integration was used to illustrate how these effects influence the ZVS boundary conditions.

Chapters 5 and 6 exploit the potential of these universal ZVS boundary conditions to extend the commonly used (inherent and/or external) single series impedance model to a more complex AC coupling network with multiple impedance parameters. This investigation shows how a deliberately reduced transformer coupling expands the ZVS region at constrained operating points to achieve continuous
ZVS operation. This chapter then continues to illustrate that an adaptive 3-level modulation concept can be used to maintain the quantified transformer coupling coefficient as high as possible, while increasing the additional RMS circulating currents only as much as is required to benefit from the additional magnetising current and maintaining highest possible conversion efficiency. The proposed design and operation strategy has been applied to an experimental DAB test system to confirm the validity of the approach, and then implemented on a customised DAB prototype for overall efficiency evaluation (96.5% - 98.5%) in the entire operating range.

**Chapters 7 and 8** extend the frequency domain analysis to also accommodate the DC bus currents. After identifying the practical issues in the DC bus filter design that can lead to harmonic problems, these chapters analytically derive the magnitude and frequency of the DC bus harmonic current components for any DC-DC bus voltage ratio and power transfer conditions. This analysis is then used to identify how adaptive 3-level modulation can be included into the filter design process, to actively shape the DC bus current and thus selectively suppress particular harmonic components that cause critical frequency resonance DC bus oscillations. This allows the filter capacitor size to be set to the minimum value required to support the bridge switching transitions.

## 10.2 Future Work

This section lists future work topics related to Dual Active Bridge DC-DC converters. Generally, it can be expected that the need for advanced impedance modeling will further increase with the operating frequencies. The presented frequency domain analysis technique establishes a powerful framework to accommodate such detailed impedance models, including parasitic coupling impedances in the AC link or DC bus connection. Some ideas for further work in this research area are mentioned in the following:

### 10.2.1 Precise Modeling of Parasitic AC Coupling Impedances

This thesis has analysed monotonic AC link impedances. However, as switching frequencies increase, other transformer design technologies such as planar PCB-integrated windings become more attractive. To precisely analyse the implications of such a winding technique for a DAB, it becomes more and more relevant to include the impact of the parasitic transformer capacitance and bridge-to-transformer connecting impedances to evaluate their impact on the DAB performance. For planar transformers in

![Figure 10.1: Intra-winding capacitance of HF transformer](image-url)
particular, the winding layers are located in close proximity and can hence cause the intra-winding and inter-winding capacitance to increase substantially.

A significant intra-winding capacitance is expected to suppress those integer harmonic frequencies that are located beyond to the transformer resonance frequencies. If these harmonic orders are small integer harmonics of the fundamental switching frequency, the capacitance has a significant effect on the power transfer and ZVS range capability. Also, the effective switched phase leg capacitance can become significantly greater than the total switch device output capacitance, which increases the amount of circulating current required at the switching transition to achieve complete ZVS. Fig. 10.1 shows the equivalent circuit diagram of a transformer including the parasitic intra-winding capacitances.

It is commented here that the presented work has applied frequency domain analysis to the differential mode operation of a DAB converter. However, for a high voltage DC bus with substantial capacitive coupling to ground and high-frequency operation, the generation of common-mode voltage harmonics (particularly emphasized by 3-level adaptive modulation) can cause additional circulating currents through the transformer inter-winding capacitance. This can significantly affect the DAB performance unless passive common-mode filters and/or circulating common-mode loops are included.

10.2.2 Multi-Port DAB Converters

Multi-port DAB concepts have already been proposed in literature [136] - [139] and offer an attractive solution to manage the power flow between multiple (three or more) DC sources. However, the analysis complexity for simultaneously transferring power between multiple DC ports significantly increases. Fig. 10.3 shows such a multi-port (single phase) DAB circuit topology. The converter may only include one single transformer core element with multiple coils connecting the transformer to the respective converter bridges. This topology can be beneficial to transfer power between multiple DC bus voltage levels and thus reduce the number of conversion stages that would conventionally be required. Frequency domain analysis is inherently capable to include the increased design and modulation complexity of such a topology. Note that two control degrees of freedom are added with every additional full bridge which can be used in order to maintain maximum converter performance as operating conditions vary. For the exemplar case of a three-port DAB network, the modulation analysis is extended to include three full bridge duty cycles $\alpha$, $\beta$, $\gamma$ and two phase shift angles $\delta_1$ and $\delta_2$, while they are opposed to two independent DC-DC bus ratios $d_1$ and $d_2$.

Alternatively, an additional DC bus switch element can be located between each converter bridge and the main DC bus storage element (i.e. bus capacitor) to isolate the DC bus from the AC coupling network. This way, if one DC output is not active as source or load, its cross-interaction with the remaining circuit can be interrupted because the bridge diodes can no longer be forward biased at any operation condition.
Figure 10.2: Multi-port (single phase) DAB topology

10.2.3 Variants of DAB Circuit Topology

Circuit variations from the conventional DAB converter have been widely reported in literature [140] [141], also impacting on the modulation strategy. For example, the reduction of one bridge circuit from two to one phase leg using balancing DC bus capacitors (“voltage doubler”) [142] reduces the count of available control angles by one, while a circuit extension to a T-type [143] or three-level NPC-type [144] H-bridge adds control degrees of freedom into the modulation scheme. Such topology and control modifications can be analysed following the same approach as presented in this thesis.

10.2.4 Advanced Design of DC Bus Filter

This work has precisely determined the DC bus harmonics for single and three-phase DAB converters. These results and the outlined correlations between the DC bus frequency components and the bridge modulation parameters now allow for advanced filter design strategies to be explored, recognising that the filter volume can significantly contribute to the total size and cost of a DAB.

10.2.5 Closed Loop Control

In this thesis, the DAB modulation parameters have been calculated offline for each operating condition using harmonic summation development, and then forwarded to the gate driver ICs by the DSP. Such a look-up table typically suffers from a low robustness against transient disturbances and component (lifetime) tolerances. Hence, in practice, a feedback loop is required where the phase shift $\delta$ is selected as closed loop control angle $\Delta angle$ and added to the feedforwarded (single phase) DAB angle parameters ($\alpha, \beta, \delta$). The effective modification of $\delta$ in steady-state operation depends on impedance tolerance deviations and other second-order effects such as a DC bus voltage ripple. These uncertainties need to be incorporated in the design process since it may otherwise cause e.g. undesired hard switching.
A cascaded PI control loop is shown in Fig. 10.4. An inner current feedback loop with a parallel feedforward gain sets the DC bus current reference requested by the outer PI voltage controller output.

Similarly, for a three-phase DAB, the proposed asymmetric three-phase DAB modulator scheme to compensate for unbalanced three-phase transformer impedances needs to be implemented in closed loop configuration to automatically adjust the feedforwarded angle parameters to achieve sufficient control dynamics.
Appendix A: Online AC Link Impedance Detection using Practical Dead-Time Impact

In Chapter 3, the ZVS boundaries of a single phase DAB were precisely determined for any coupling impedance, while taking into account the non-ideal switching effects of device charge and dead-time. Fig. 3.13 shows that evaluating the phase leg current polarity at the end of dead-time would theoretically extend the ZVS operation for \( d \geq 1 \) and \( \delta \leq 0 \) (primary bridge), and for \( d \leq 1 \) and \( \delta \geq 0 \) (secondary bridge) by a small region. Within this region, the phase leg current through the anti-parallel diode of the turned OFF switch moves towards zero magnitude. If the load current does not reach zero within the dead-band, the opposing active switch element is hard turned ON. If the load current however reaches zero within this interval, the load current will naturally commutate to the opposing diode to initiate the phase leg voltage transition. This can be effectively referred to as Zero Current Switching (ZCS). For both hard and ZCS transition, the commanded phase shift angle \( |\delta|_{\text{cmd}} \) will be smaller than the physically applied phase shift angle \( |\delta| \). This deviation reduces the closer the operating condition gets to the actual ZVS boundary until it eventually reaches this limit, and \( |\delta| \) equals \( |\delta|_{\text{cmd}} \). Fig. A.1 shows this process as the commanded phase shift value \( |\delta|_{\text{cmd}} \) increases within the indicated dead band, while the effective phase shift \( |\delta| \) and thus the actual operating condition (i.e. transformer current) remains the same. This stagnation only relases after the dead band has been passed ("phase jump"), i.e. the phase leg current has the right polarity for ZVS at the initial turn OFF instant.

This stagnation effect and the definition of the ZVS boundaries can now be used to precisely char-

![Figure A.1: Phase shift stagnation during dead band and subsequent phase jump (d = d_{ZVS} = \text{const.})](image-url)
acterise the AC coupling impedance of a DAB. As an application example, the offline measurements of the HF transformer impedances (T1-T4 in Table 3.1.) can be verified during actual converter operation. The dead-time angles of the primary and secondary converter bridge are set to 2.3 $\mu$s (i.e. $\rho_{DT_p} = 0.29$ rad for a 20 kHz switching frequency).

The ZVS boundary condition of the primary and secondary bridge is detected as the commanded phase shift angle $\delta$ increases from zero to move the DAB from the hard switching region (diode-to-switch commutation) via the boundary condition (diode-to-diode commutation) into ZVS (switch-to-diode commutation). The “phase jump” occurs when the phase leg current passes zero right after device turn-OFF at the ZVS boundary condition (i.e. a certain couple of phase shift $\delta_{ZVS}$ and DC-DC bus voltage ratio $d_{ZVS}$). Following this principle, multiple ZVS boundary conditions can be detected for a wide variation of the DC-DC bus voltage ratio and phase shift angles. Fig. A.2 shows a good match between the experimentally detected boundary points and the ZVS boundary curves using the impedance measurements in Table 3.1. A separate FEA calculation of these impedances has also been carried out to further confirm this approach. As the boundary conditions are always detected just after entering ZVS they occur for slightly higher values of $|\delta|$ than expected by the theoretical ZVS boundary curve. Figs. A.3 and A.4 show the experimental waveforms (T1-T4) for the marked operating points in Fig. A.2 ($\delta = \pm 0.4$ rad). It is commented that there is a slight negative DC bias current offset in the measurement of $i_p$ and a positive DC offset in $-i_s$.

Such an online impedance detection can be conducted during the ramp-up of a DAB. This allows a very precise determination of the AC coupling network, required for optimal and safe operation, since it evaluates these embedded impedances inside their final converter environment. This detection method can run at very low power transfer levels, which ensures that no harm is caused to the converter as the

![Figure A.2: Comparison of online ZVS impedance detection with offline impedance measurements](image-url)
Figure A.3: Experimental waveforms ($\delta = 0.4$ rad, $2V_{p,DC} = 100V$) at secondary bridge ZVS limits

Figure A.4: Experimental waveforms ($\delta = -0.4$ rad, $2V_{p,DC} = 50V$) at primary bridge ZVS limits

parameters of the coupling impedance are still unknown to the controller.

This method can also be applied to inductive power transfer (IPT) systems to accurately determine the coupling-coefficient prior to nominal operation. In this case, the DAB could be operated at higher (than nominal) switching frequencies to avoid harmful AC link current magnitudes at resonance frequency.
Appendix B: 3-Level Cusp Modulation Angles for Lossless DAB AC Coupling Impedance

The 3-level modulation angles ($\alpha_{cusp}$ for $d < 1$ and $\beta_{cusp}$ for $d > 1$) required to maintain continuous ZVS operation at a particular DC-DC bus voltage ratio $d$ and power transfer as solution to (5.14) and (5.18) become

$$\alpha_{cusp} = \frac{4(\chi - 1)\rho_{DT_p} - 2(\chi - 1)(A_6 - d_{\min}\pi[1 - 2\chi]) - A_2 + d_{\min}2\pi A_3 + A_5 A_1}{4(\chi - 1)}$$

$$+ \sqrt{\left( A_1 \right)^2 + \frac{-4(\chi - 1)\rho_{DT_p} (A_6 - d_{\min}\pi[1 - 2\chi]) - A_2 (A_6 - d_{\min}\pi[1 - 2\chi])}{2(\chi - 1)}}$$

$$A_1 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [2\chi(1 - \chi)] \quad A_2 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [2\chi(1 - \chi)] \quad A_3 = [1 - 2(1 - \chi)]$$

$$A_4 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [1 - 2\chi(1 - \chi)] \quad A_5 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [2\chi(1 - \chi)] \quad A_6 = \frac{\Delta_{ipsw} L}{V_{p,DC}} [1 - 2\chi(1 - \chi)]$$

$$\beta_{cusp} = \frac{2\pi(B_3 - B_4) + B_5 + (1 - 2\chi)(B_1 + B_2)}{4d_{\max}^2}$$

$$+ \sqrt{\left( \frac{2\pi(B_3 - B_4) + B_5 + (1 - 2\chi)(B_1 + B_2)}{4d_{\max}^2} \right)^2 - \frac{B_2(B_3 - B_4) + (B_1 + B_2)(\pi + B_6)}{d_{\min}^2 \chi^2} \pi}$$

$$B_1 = 2\pi(\chi - 1)(1 - \frac{\rho_{DT_p}}{\pi}) \quad B_2 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [2\chi(1 - \chi)] \quad B_3 = [1 - 2(1 - \chi)] \pi(1 - \frac{2\rho_{DT_p}}{\pi})$$

$$B_4 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [1 - 2\chi(1 - \chi)] \quad B_5 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [2\chi(1 - \chi)] \quad B_6 = \frac{\Delta_{ipwsw} L}{V_{p,DC}} [1 - 2\chi(1 - \chi)]$$
Appendix C: N87 Ferrite Core Loss Estimation Using IGSE

The Steinmetz Equation defines the per volume hysteresis core loss $P_c$ (in kW/m$^3$), as a function of the particular harmonic frequency of excitation and peak flux density, as follows:

$$P_c = k_c f^\alpha_c B^\beta_c \quad (C.1)$$

where $k_c$, $\alpha_c$ and $\beta_c$ are the three material-specific Steinmetz parameters. Curve fitting between the measured loss data and (C.1) can be used to define their values. The Steinmetz Equation does not account for temperature variations. Thus, the N87 Steinmetz parameters are separately defined for 25°C and 100°C:

- $\alpha_{c(25^\circ C)} = 1.55$, $\beta_{c(25^\circ C)} = 2.95$, $k_{c(25^\circ C)} = 0.8542$ and $\alpha_{c(100^\circ C)} = 1.29$, $\beta_{c(100^\circ C)} = 2.37$, $k_{c(100^\circ C)} = 10.8564$.

$P_c$ is linearly interpolated between the two selected temperature points to evaluate the core loss at the operated core temperature. Fig. C.1 shows the match between the interpolated and the actually measured core power loss characteristic [128].

However, the AC link current waveforms in a DAB contain significant higher-order harmonic current components. The Generalised Improved Generalised Equation (IGSE) can be reduced (with a deviation of less than 0.15% if $0.5 \leq \alpha_c \leq 3$ [62]) to give

$$P_c = \frac{k_i \Delta B^{\beta - \alpha}}{T_{sw}} \int_0^{T_{sw}} \left| \frac{dB}{dt} \right|^\alpha dt \quad (C.2)$$

where $T_{sw} = \frac{2\pi}{w_{sw}}$ is the fundamental switching period and $k_i$ is defined as

$$k_i = \frac{k}{(2\pi)^{\alpha-1}} \int_0^{2\pi} \left| \cos \theta \right|^{\alpha 2^\beta - \alpha} d\theta \approx \frac{k}{2^{\beta+1} \pi^{\alpha-1} (0.2761 + \frac{1.7032}{\alpha+1.354})} \quad (C.3)$$
Figure C.1: Curve fitting for EPCOS N87 ferrite material
Appendix D: MATLAB Code Example - Minimisation of Particular DC Bus Harmonic

```matlab
clear; clc;

%% Set operation point...
Vpdc = 0.5*50; % Input voltage
d = 0.8;

for p = 1:1:6 % vary active battery power
    Pp = 5 + p*15;

    % Reference DC battery current
    Ipdc_Ref = Pp/(2*Vpdc);

%% Practical Switching Impact

%% Min. Circulating Current
Delta_ip = 0;
Delta_is = 0;

%% Switching Frequency
fs = 20e3;
ws = 2*pi*fs;

%% AC Link Impedances
trafomodel = 'RL';

if (trafomodel == 'RL')
    % Coupled inductor
    R = 400e-3;
    L = 103e-6;
```
else
  % Transformer
  ... 
end

%% Initialize ...

% Resolution of angles
prec_delta = 200;
prec_alpha = 100;
prec_beta = 1;

% Initialize dc current
Ipdc_sum = zeros(prec_delta, prec_alpha, prec_beta);

Nmax = 20; % maximum number of harmonics

%% Power Flow Direction ( for range of delta )
if (Pp>=0)
  pwr_sgn = 1;
else
  pwr_sgn = -1;
end

%% Step through all combinations of alpha, beta and delta
for r = 1:1:prec_delta % vary delta
  dc_harmonic_opt(r) = inf; % Set minimum dc bus harmonic current magnitude to infinity for every iteration of delta
  dc_harmonic_opt_2VS(r) = inf;
  delta_opt(r) = inf;
  alpha_opt(r) = inf;
  beta_opt(r) = inf;
  delta = pwr_sgn * r*pi/2/prec_delta;

  for l = 1:1:prec_alpha % vary alpha
    alpha = 2*pi/l/3 + 1/prec_alpha*pi/3;
    for s = 1:1:prec_beta % vary beta
beta = s/prec_beta*pi; %pi

%%
c = zeros(1,18); % set each dc current harmonic summation ...to zero

%% reset ZVS sums to zero...

% HB1
sum_A_HB1= 0; sum_B_HB1= 0; sum_C_HB1= 0; sum_D_HB1= 0; sum_E_HB1= 0;

% HB2
sum_A_HB2= 0; sum_B_HB2= 0; sum_C_HB2= 0; sum_D_HB2= 0; sum_E_HB2= 0;

% HB3
sum_A_HB3= 0; sum_B_HB3= 0; sum_C_HB3= 0; sum_D_HB3= 0; sum_E_HB3= 0;

% HB4
sum_A_HB4= 0; sum_B_HB4= 0; sum_C_HB4= 0; sum_D_HB4= 0; sum_E_HB4= 0;

%% Number of calculated harmonics...

for n = 1:1:Nmax % vary max. number of harmonics

%% Calculation of RMS in this OP

% Primary side converter harmonics
Vp_base = 4*Vpdc/pi;
Vp_complex = ...
    Vp_base/(2*n-1)*(exp(j*(2*n-1)*alpha/2)-exp(j*(2*n-1)*(-alpha/2)));

% Secondary side converter harmonics
Vs_base = 4*d*Vpdc/pi;
Vs_complex = ...
    Vs_base/(2*n-1)*(exp(j*(2*n-1)*(beta/2-delta))-exp(j*(2*n-1)*(-beta/2-delta)));

%% Primary Current: Impedance Matrix Element

if (trafomodel == 'RL')

%%RL coupled inductor
    yp_p = 1/(R + j*(2*n-1)*ws*L);
    yp_s = -1/(R + j*(2*n-1)*ws*L);

else
%Actual transformer

\[
yp_s = -j*(2*n - 1)*ws*Lm/(-(Lp+Ls)*Lm+ Lp*Ls)*((2*n-1)*ws)^2 + ... \\
(Lp*Rs + Ls*Rp + Lm*(Rp+Rs))*j*(2*n-1)*ws + Rp*Rs);
\]

\[
yp_p = -yp_s*(((Lm+Ls)*j*(2*n-1)*ws + Rs)/(Lm+j*(2*n-1)*ws));
\]

end

Ip_complex = yp_p * Vp_complex + yp_s * Vs_complex;
Ip = abs(Ip_complex);
thetap = angle(Ip_complex);

%% Secondary Current: Impedance Matrix Element

if (trafomodel == 'RL')
  %RL
  ys_p = -1/(R + j*(2*n - 1)*ws*L);
  ys_s = 1/(R + j*(2*n - 1)*ws*L);
else
  %LLL
  ys_p = -j*(2*n - 1)*ws*Lm/(-(Lp+Ls)*Lm+ Lp*Ls)*((2*n-1)*ws)^2 + ... \\
(Lp*Rs + Ls*Rp + Lm*(Rp+Rs))*j*(2*n-1)*ws + Rp*Rs);
  ys_s = -ys_p*(((Lm+Lp)*j*(2*n-1)*ws + Rp)/(Lm+j*(2*n-1)*ws));
end

Is_complex = ys_p * Vp_complex + ys_s * Vs_complex;

%% Calculate average dc bus current and magnitude of dc bus current harmonic

Ipdc(n+1) = 2/pi/(2*n - 1)*sin((2*n - 1)*alpha/2)*sin(thetap)*Ip;
Ipdc_sum(r,l,s) = Ipdc(n+1) + Ipdc_sum(r,l,s);

for k = 2:2:18
  % Real Part of rectifying function
  re_h = ... \\
  2/(pi*(k^2-(2*n-1)^2))^2*(k+(2*n-1))*sin(thetap)*sin(alpha/2*(k-(2*n-1)))+ ... \\
  (k-(2*n-1))*sin(thetap)*sin(alpha/2*(k+(2*n-1))));

  % Imaginary Part of rectifying function
  imag_h = ...
  2/(pi*(k^2-(2*n-1)^2))^2*(k+(2*n-1))*cos(thetap)*sin(alpha/2*(k-(2*n-1)))- ...


\[(k-(2*n-1))\times \cos(\text{thetap})\times \sin(\alpha/2\times (k+(2*n-1))))\];

\%

Gain and Phase of rectifying function

\[
\begin{align*}
\text{abs}_h &= \sqrt{\text{re}_h^2 + \text{imag}_h^2}; \\
\text{phi}_h &= \text{angle}(\text{re}_h + j\times \text{imag}_h);
\end{align*}
\]

\%

dc link harmonic

\[
\text{c}_\text{add}(k) = Ip\times \text{abs}_h\times \exp(j\times \text{phi}_h); \quad \text{% to each odd ...}
\]

ac link harmonic m there are even dc link harmonics 0..2..4...

\[
\text{c}(k) = \text{c}(k) + \text{c}_\text{add}(k); \quad \ldots
\]

\%

each dc link harmonic is summed up

end

\%

ZVS Detection in this OP (...) % calculate ZVS summation terms for each ...

phase leg

end

\%

ZVS

\[
\begin{align*}
\text{du1}(r,l,s) &= (\text{sum}_A\_HB1 + \text{sum}_B\_HB1 + \text{sum}_C\_HB1 - \ldots) \\
&\pi\times \text{Delta_ip}/(4\times Vpdc)/(2\times (\text{sum}_D\_HB1 + \text{sum}_E\_HB1)); \\
\text{du2}(r,l,s) &= (\text{sum}_A\_HB2 + \text{sum}_B\_HB2 + \text{sum}_C\_HB2 + \ldots) \\
&\pi\times \text{Delta_ip}/(4\times Vpdc)/(2\times (\text{sum}_D\_HB2 + \text{sum}_E\_HB2)); \\
\text{dl3}(r,l,s) &= (2\times (\text{sum}_A\_HB3 + \text{sum}_B\_HB3) + \ldots) \\
&\pi\times \text{Delta_is}/(4\times Vpdc)/(\text{sum}_C\_HB3 + \text{sum}_D\_HB3 + \text{sum}_E\_HB3); \\
\text{dl4}(r,l,s) &= (2\times (\text{sum}_A\_HB4 + \text{sum}_B\_HB4) + \ldots) \\
&\pi\times \text{Delta_is}/(4\times Vpdc)/(\text{sum}_C\_HB4 + \text{sum}_D\_HB4 + \text{sum}_E\_HB4);
\end{align*}
\]

\[
\begin{align*}
\text{alpha}_\text{tmp}(r,l,s) &= \alpha; \\
\text{beta}_\text{tmp}(r,l,s) &= \beta;
\end{align*}
\]

\%

Checks

\%

cHECK power requirement (i.e. average dc bus current) for given delta

if (abs((Ipdc\_sum(r,l,s)-Ipdc\_Ref)/Ipdc\_Ref) <= 1.5e-2)

\%

check magnitude of dc bus harmonic component of interest (here: 18th harmonic)

\[
\text{dc}_{18h}(r,l,s) = \text{abs}(\text{c}(18));
\]

if (\text{dc}_{18h}(r,l,s) < \text{dc}_{harmonic\_opt}(r)) % overwrite angles only ... if dc harmonic magnitude is reduced for this delta, ...
otherwise next delta

dc.harmonic_opt(r) = dc.18h(r,l,s);

alpha_opt(r) = alpha_tmp(r,l,s);

beta_opt(r) = beta_tmp(r,l,s);

else
end

% check ZVS in all half bridges (if wanted)

if (d < du1(r,l,s) && d < du2(r,l,s) && d > dl3(r,l,s) && d > dl4(r,l,s))

% 18th harmonic

dc.18h.ZVS(r,l,s) = abs(c(18));

% choose harmonic of interest, e.g. dc bus parasitic resonance frequency

if (dc.18h.ZVS(r,l,s) < dc.harmonic_opt.ZVS(r)) % overwrite ...

% angles only if dc harmonic improved is achieved for this ...

% delta, otherwise next delta

dc.harmonic_opt.ZVS(r) = dc.18h.ZVS(r,l,s);

alpha_opt.ZVS(r) = alpha_tmp(r,l,s);

beta_opt.ZVS(r) = beta_tmp(r,l,s);

else
end

else

dc.18h.ZVS(r,l,s) = NaN;
end

end

beta_(s) = beta;

end

alpha_(l) = alpha;

end

delta_(r) = delta;

end

% Evaluation (Best valid OP across whole range)

[min_value,min.index2] = min(dc.harmonic_opt.ZVS); % min.value is the ...

minimum RMS current and according delta

if (min_value == inf)

dc.harmonicOpt.ZVS(p) = NaN;

alphaOpt_ZVS(p) = NaN;
betaOpt_ZVS(p) = NaN;
deltaOpt_ZVS(p) = NaN;

else
dc_harmonicOpt_ZVS(p) = min_value;
alphaOpt_ZVS(p) = alpha_opt(min_index2);
betaOpt_ZVS(p) = beta_opt(min_index2);
deltaOpt_ZVS(p) = delta_(min_index2);
end

Pp_(p) = Pp;

end

%% 2D Plot across operating power range at given voltage ratio

plot(Pp_(˜isnan(alphaOpt_ZVS(:))),alphaOpt_ZVS(˜isnan(alphaOpt_ZVS(:))),'b+'); hold all;
plot(Pp_(˜isnan(betaOpt_ZVS(:))),betaOpt_ZVS(˜isnan(betaOpt_ZVS(:))),'rs'); hold all;
plot(Pp_(˜isnan(deltaOpt_ZVS(:))),deltaOpt_ZVS(˜isnan(deltaOpt_ZVS(:))),'go'); hold all;
%plot(Pp_(˜isnan(dc_harmonicOpt_ZVS(:))),dc_harmonicOpt_ZVS(˜isnan(dc_harmonicOpt_ZVS(:))),'k'); ...
hold all;

xlabel('Power in W');
legend('alpha','beta','delta');
xlim([0 100]);
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